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A Digital Intermediate Frequency Receiver for Inter-vehicle Communications

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***Abstract*—This paper proposes a digital intermediate frequency (D-IF) receiver for inter-vehicle communications. Bandpass sampling is employed to lower the sampling rate. Appropriate selection of sampling rate and equivalent digital IF frequency results in a simplified Digital down converter (DDC). Meanwhile, the simplified DDC makes the combination of DDC and the following low pass filter (LPF) possible. This combination reduces the complexity. Unique word (UW) correlation is used to perform frame detection and frequency offset estimation. Finally, a Turbo decoder is employed to provide enough coding gain for combating fading.**

I. INTRODUCTION

DEDICATED short-range communication system (DSRC) standard [1] based Inter-vehicle communications (IVC) system plays a key role in Intelligent Transportation System (ITS). Inter-vehicle communications provide many important and useful applications such as collision avoidance, real-time traffic information relay and sharing, and entertainment applications.

DSRC based IVC systems are projected to operate around 5.8GHz in a high-speed mobile environment with communication distance of up to 400 meters. Multipath fading shall be taken into consideration for such environments. The typical fading model for IVC channels is the Rician model as strong line of sight (LOS) components exist [2]-[4]. The degradation due to Rician multipath fading for $\pi/4$ DQPSK, the modulation scheme adopted in DSRC standard, is about 5 to 10dB for a typical Rician factor around 10dB in IVC channels [5]. Therefore, some kind of forward error correction (FEC) code is necessary to combat fading.

A digital intermediate frequency (D-IF) receiver based on bandpass sampling is proposed for IVC system. There are several attributes of this D-IF receiver: Firstly, the bandpass sampling technique is employed to lower the sampling rate and reduce the power consumption. Secondly, appropriate selection of sampling rate and equivalent IF frequency results in simplified Digital down converter (DDC). With the simplified DDC, the combination of DDC and following low pas filter (LPF) can be exploited to reduce complexity [6]. Thirdly, unique word (UW) correlation is used to perform frame detection and frequency offset estimation. This data aided frequency offset estimation and correction algorithm is sufficient to handle the large frequency offset (40 ppm/232kHz or 40.78 degrees) of DSRC IVC systems. Finally, a Turbo decoder is employed and the coding gain is more than 10dB for the bit error rate (BER) of 10^{-5}. This gain shall be enough to counter multipath fading in IVC channels.

The rest of the paper is organized as follows: Section II introduces a brief overview of DSRC IVC systems. Section III presents the proposed DSRC IVC D-IF receiver. Several major building blocks such as the bandpass sampler, DDC and LPF, timing estimation, frequency estimation and Turbo decoder are discussed in detail. Simulation results are shown in Section IV. Section V discusses FPGA evaluation briefly. Finally, conclusions are summarized in Section VI.

II. DSRC IVC OVERVIEW

Figure 1 shows the physical layer data frame structure of the DSRC IVC system. Each frame starts with the 128 bit preamble and the 16 bit UW. 792 bit of data is contained in each frame. Timing estimation and synchronization can be done during the PR period and the UW can be used for frame detection and frequency offset estimation. Major parameters of DSRC IVC systems are listed in Table 1.

PR(128)	UW (16)	Data (792)

Fig. 1. DSRC Physical Layer Frame Structure

TABLE1
MAJOR PARAMETERS OF IVC SYSTEM

Parameters	Values
Frequency	5.8GHz
Modulations	$\pi/4$ DQPSK
Symbol Rates	2.048M
Pulse Shaping	Raised Cosine Filter, roll-off factor of 1
Multiple Access	TDMA-FDD

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Bandwidth	5.0MHz
BER Requirement	10^{-5}
Frequency Stability	Base Station: 20ppm Mobile Station: 20ppm

III. PROPOSED SCHEME

Figure 2 presents the block diagram of DSRC IVC D-IF with a Turbo decoder. Combined DDC and LPF perform baseband signal recovery and out-of-band noise rejection. The timing estimation circuit estimates the correct sampling time and determines the sampling signals to be used for the following processing. Several kinds of tasks such as phase detection; differential decoding, UW correlation, frequency estimation and correction are conducted in the frequency module. Also, a UW detection flag signal is sent back to the timing estimation block to control the timing estimation duration: The timing estimation duration will be changed from 32 symbols to 64 symbols after UW detection. This adjustment is mainly for improving timing estimation accuracy during the data reception period. Finally, soft decision output from the frequency module is sent to the Turbo decoder for decoding and the hard decision output will be generated after certain number of decoding iterations.

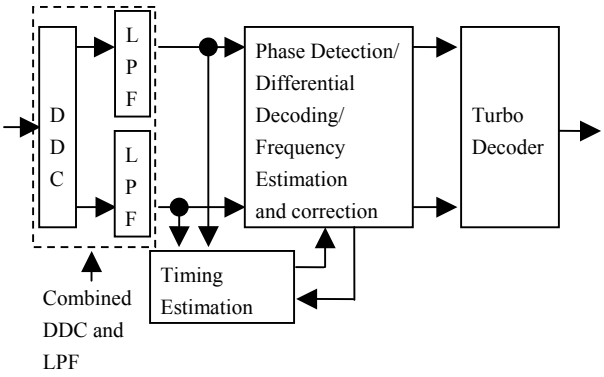


Fig. 2. Block Diagram of DSRC IVC D-IF

Detailed descriptions of each major module are as follows:

A. Bandpass Sampling

Bandpass sampling technique becomes popular in D-IF receivers. The main driving force is to reduce the power consumption by using low sampling rates. With bandpass sampling, the sampling rate can be lower than the IF frequency as long as it is higher than twice the bandwidth of the wanted signal. In other words, bandpass sampling oversamples the wanted signal while it undersamples the IF signal. The sampling rate of the bandpass sampling shall meet the following requirement [7]:

$$2f_U / n \le f_S \le 2f_L /(n-1), 1 \le n \le \lfloor f_U / B \rfloor. \quad (1)$$

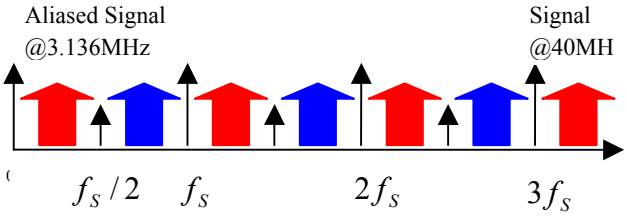
Where f_U is the highest frequency of IF signal, f_L is the lowest frequency of IF signal, f_S is the sampling rate, B is the occupied bandwidth of IF signal, and n is an integer number.

Table 2 lists the possible sampling rate range for the proposed system with the IF frequency of 40MHz, the bandwidth of 5MHz and the symbol rate of 2.048M.

TABLE2
POSSIBLE SAMPLING RATES FOR THE SYSTEM

n	f_S (MHz)	f_S in terms of oversampling rate over the symbol rate
2	[42.5 75]	[21X 36X]
3	[28.33 37.5]	[14X 18X]
4	[21.25 25]	[11X 12X]
5	[17 18.75]	9X
6	[14.17 15]	7X
7	[12.14 12.5]	6X
8	[10.63 10.7]	NA

Therefore, the lowest sampling rate equals an integer-number multiple of the symbol rate shall be 12.288MHz (6X). The equivalent digital IF frequency after sampling is (40-3* f_S)=3.136MHz. Figure 3 illustrates the spectrum after sampling.



Red: 3.136MHz,,15.424MHz, 27.712MHz, and 40MHz
Blue: 9.152MHz, 21.440MHz, and 33.728MHz

Fig. 3. Spectrum after Bandpass Sampling

B. DDC and LPF

Digital down conversion (DDC) is used to recover the in-phase (I) and quadrature (Q) signal envelopes from the IF signal. The complexity of DDC could be simplified by choosing a proper IF frequency and sampling rate. For example, if the sampling rate is 4 times the IF frequency,

the sine and cosine signals that represent the complex phasor degenerate to two simple sequences of [1 0 -1 0...] and [0 -1 0 1...]. Please note the equivalent digital IF frequency (3.136MHz) for DSRC IVC D-IF based on bandpass sampling is not equal to one fourth of the sampling rate (3.072MHz). Therefore, the simplified DDC structure cannot be used directly. However, it is possible to use the simplified DDC design without modification by forcing the digital IF frequency of the DDC to be one fourth of the sampling rate, i.e., 3.072MHz. The penalty is that an extra frequency offset of -64kHz is introduced. This extra frequency offset can be compensated before frequency estimation, as it is a fixed frequency offset.

A LPF is used to remove higher frequency components and out-of-band noise. The combination of DDC and LPF is possible because a simplified DDC structure is employed. This combination will halve the complexity of the LPF [6].

C. Timing Estimation

The square timing recovery algorithm [8] is employed to perform timing estimation and correction. The Discrete Fourier transform (DFT) is applied to the squarer output to obtain the timing information.

Suppose the received complex symbol $r(t) = I(t) + jQ(t)$ is sampled at the rate of N/T, where T is the symbol interval and N is the oversampling rate, and then the amplitude of the squared received symbol is:

$$x(t) = |r(t)|^2 = |I(t)|^2 + |Q(t)|^2 . \quad (2)$$

The samples of x(t) are:

$$x_k = x(kT/N), \quad k = 0,1,..... \quad (3)$$

The amplitude contains a spectral component at $1/T$ or the symbol rate, which can be determined by computing the complex Fourier coefficient at the symbol rate over a period equivalent to LN samples (L is the number of symbols used for the estimation):

$$X_m = \sum_{k=mLN}^{(m+1)LN-1} x_k e^{-j\frac{2\pi k}{N}} . \quad (4)$$

It has been proven that $-1/2\pi \bullet \arg(X_m)$ is the unbiased estimation of the timing offset.

Due to the small oversampling rate (6X); an interpolator is indispensable to obtain good performance. When the symbol timing is determined at somewhere between the two adjacent samples, a simple 2-point Lagrange interpolator is used to obtain an estimated value at the estimated sampling time.

Normally timing estimation is performed over a certain number of symbols. The reliability of the timing offset estimation is improved with larger number of symbols. However, stable timing estimation can be only obtained after at least two estimation cycles. Therefore, the optimal timing estimation period before UW is 32 symbols as the length of PR is 64 symbols. On the other hand, to achieve the accurate timing estimation result during the data reception period, the timing estimation period shall be increased. Considering the trade-off between estimation accuracy and processing latency, the timing estimation period after UW detection is set to be 64 symbols.

D. Phase Detection

To reduce the complexity of the following processing, phase detection is introduced. With phase detection, differential detection can be performed by one real subtraction instead of one complex multiplication. Also, the complex multiplication operations in UW correlation, frequency offset estimation and correction can be replaced by real subtraction operations. The cost is only a small look up table (LUT) in hardware implementation.

E. Frequency Estimation

After differential detection, the phase difference between the k^{th} and the $(k-1)^{th}$ received symbol is

$$\Delta\varphi_k = 2\pi\Delta f T_S + \Delta\phi_k , \quad (5)$$

where $\Delta\phi_k$ is determined by the modulated signal at symbol k and T_S is the symbol time duration.

Then the phase offset resulting from the frequency offset is expressed as:

$$2\pi\Delta f T_S = \Delta\varphi_k - \Delta\phi_k . \quad (6)$$

Good $\Delta\phi_k$ estimation can be obtained by hard decision if the frequency offset is smaller than 25ppm or 25 degrees. Unfortunately, the phase offset is quite big in DSRC IVC applications. Sometimes it can be as big as 40.78 degrees or 40ppm. Therefore, accurate $\Delta\phi_k$ cannot be obtained by estimation based on hard decisions. A data aided frequency estimation algorithm should be used for initial frequency estimation. After compensating the received symbols with the estimated frequency offset, $\Delta\phi_k$ can be estimated based on hard decisions.

The known PR and UW patterns can be used to do initial frequency estimation. Firstly, PR and UW can be mapped into the phases $\Delta\phi'_k$ for k=1,…, L (L is 16 as 8 PR

symbols are included in UW correlation to reduce UW detection false alarm ratio). Then the mapped phases $\Delta\phi'_k$ will be subtracted from the differential detector outputs $\Delta\varphi_k$. The resulting phase differences between the PR & UW symbols and the differential detector outputs are:

$$\Delta\varphi_k - \Delta\phi'_k = 2\pi\Delta f\, T_s + \Delta\phi_k - \Delta\phi'_k \quad \text{k=1...L.} \quad (7)$$

If the received symbols can be matched with the known PR & UW symbols exactly, the mean of $\Delta\varphi_k - \Delta\phi'_k$ over L symbols should be equal to the phase offset $2\pi\Delta f T_s$ (Equation 8), and the corresponding mean variance should be near zero (Equation 9) since the variances are just caused by noise.

$$E\left[\Delta\varphi_k - \Delta\phi'_k\right] = \left[\sum_{k=1}^{L}\left(\Delta\varphi_k - \Delta\phi'_k\right)\right]/L \quad (8)$$

$$\sigma^2 = \left\{\sum_{k=1}^{L}\left[\left(\Delta\varphi_k - \Delta\phi'_k\right) - E(\Delta\varphi_k - \Delta\phi'_k)\right]^2\right\}/L \quad (9)$$

If the received symbols can not be matched with the known PR & UW symbols, i.e. $\Delta\phi'_k$ is different from $\Delta\phi_k$ for k=1,…,L, the mean of $\Delta\varphi_k - \Delta\phi'_k$ for k=1,…,L has no direct relations with the phase offset $2\pi\Delta f T_s$, and the corresponding mean variance will be large because the variances are caused by both noise and unmatched phase.

The mean variance in Equation 9 can be used to detect whether the received symbols are the known PR & UW or not. In other words, UW positioning or frame detection can be done by observing this mean variance. UW detection is very important as the performance of block decoding schemes such as Turbo decoding is very sensitive to the correct coding block size and position

Equation 9 can be further expressed as:

$$\sigma^2 = \frac{1}{L}\sum_{k=1}^{L}\left[\left(\Delta\varphi_k - \Delta\phi'_k\right)\right]^2 - E^2\left[\left(\Delta\varphi_k - \Delta\phi'_k\right)\right] \quad . \quad (10)$$

With Equation 10, UW detection and initial frequency offset estimation can be implemented by UW correlation. When the initial frequency offset is obtained, it will be used for initial frequency correction and the subsequent frequency estimation and correction can be done based on hard decisions. Figure 4 illustrates the frequency estimation and compensation after UW is found.

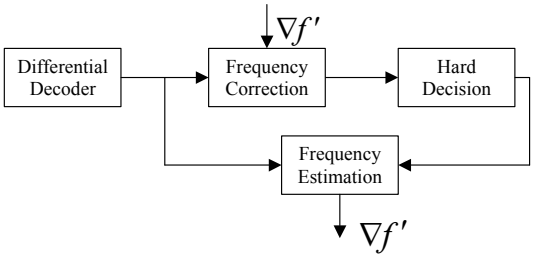


Fig. 4. Frequency Estimation and Correction based on Hard Decision

F. Turbo Decoder

The Turbo code defined in the 3GPP WCDMA specification is borrowed [9]. This Turbo coder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one Turbo code internal interleaver. The coding rate of the Turbo code is 1/3. The transfer function of the 8-state constituent code for PCCC is:

$$G(D) = \left[1, g_1(D)/g_0(D)\right], \quad (11)$$

where

$$g_0(D) = 1 + D\text{^}2 + D\text{^}3,$$
$$g_1(D) = 1 + D + D\text{^}3. \quad (12)$$

To construct the Turbo decoder, two MAP (Maximum A Posteriori) decoders with the same function as well as an interleaver and a deinterleaver are needed. These components are arranged as shown in Figure 5.

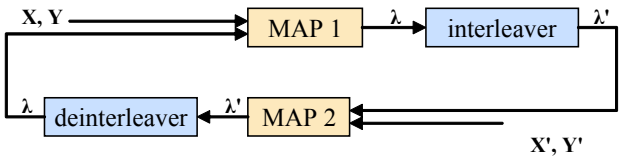


Fig. 5. Structure of the Turbo Decoder

X refers to the received systematic symbols, while Y refers to the received coded symbols. X and Y are input parameters of the first MAP decoder, while the interleaved sequence of the received bits (X' and Y') are input parameters of the second MAP decoder. Each MAP decoder computes soft likelihood values known as lambda, or λ. Note that the second MAP produces lambda values with an interleaved sequence (λ'). The hard decision, whether a bit is 0 or 1, is a function of the lambda values.

The MAP decoder is based on the modified BCJR algorithm [10], [11]. The MAX approximation

$\log(\exp(x)+\exp(y)) \approx \max(x, y)$ is used to calculate the likelihood in the LOG domain, so it is a "MAX-LOG-MAP" decoder [12].

To speed up the decoding processing, sliding window is introduced [13]. The length of the turbo decoder input is divided into smaller lengths/windows of W symbols, starting from symbols 1 to W, then $W+1$ to $2W$, and so on. If in the last frame there are remaining symbols that cannot amount to the window size W, they are grouped as another window of smaller size.

The MAP algorithm is performed on each window as if it is the full-length input size. The timing sequence of the computations of several important internal signals such as alpha (the forward likelihood values), beta (the backward likelihood values), and lambda (the extrinsic information) are illustrated in Figure 6. For example, at time $t1$, performs beta calculations from symbols $2W$ to W while alpha calculations are operated from symbols 1 to W, and the W alpha results are stored in the memory. At time $t2$, beta calculations and lambda calculations from symbols W to 1 are performed while the calculations for the next window (alpha calculation: $W \rightarrow 2W$, beta calculation: $3W \rightarrow 2W$) are run concurrently. The main idea of this timing arrangement is to avoid any delay, which is caused by waiting for alpha or beta calculations to be completed before calculating lambda, while maintaining a small window size.

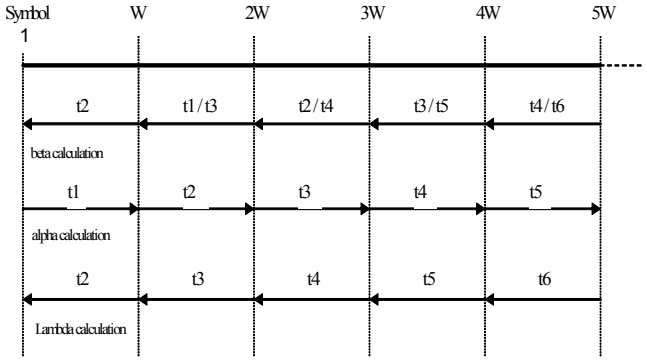


Fig. 6. Timing and Decoding Sequence Diagram with Sliding Window

IV. SIMULATION RESULTS

Simulations have been performed to evaluate the performance of the architecture presented in Figure 2. Some key parameters are listed in Table 3.

TABLE3
SIMULATION PARAMETERS

Parameter/Module	Values
Input Signal	IF of 40MHz
Sampling Rate	12.288MHz
Timing Estimation Duration	32 Symbols before UW detection; 64 Symbols after UW detection
Frequency Estimation Duration	64 Symbols
Turbo Code	3GPP WCDMA's 1/3 Turbo Code
Turbo Decoder	MAX-LOG-MAP decoder; 6 Iterations
Timing Error	Random
Frequency Offset	40ppm or 232kHz

Figure 7 shows the BER performance of the proposed DSRC IVC D-IF with a Turbo decoder. It can be observed that the BER of 10^{-5} can be achieved at Eb/No of 2.6dB. The coding gain is about 11dB.

An interesting point revealed by simulation is that the proposed frequency estimation and correction method can handle very large frequency offset such as 348 kHz/60ppm or 61.17 degrees. Figure 8 presents the BER performance with the frequency offset of 60ppm. It can be seen the degradation compared with that of frequency offset of 40ppm is very small (about 0.2dB). Therefore, the fixed frequency offset compensation for inherent frequency offset of -64kHz in the DDC is not necessary.

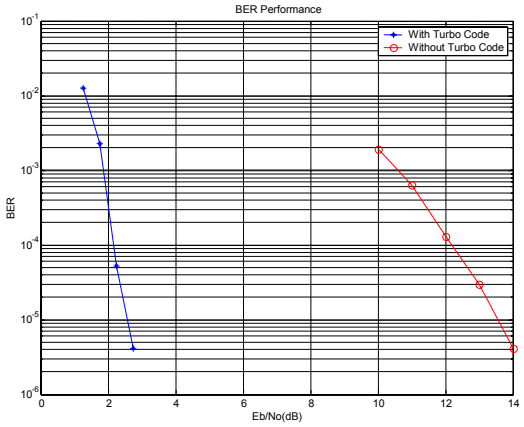


Fig. 7. BER Performance of DSRC IVC D-IF

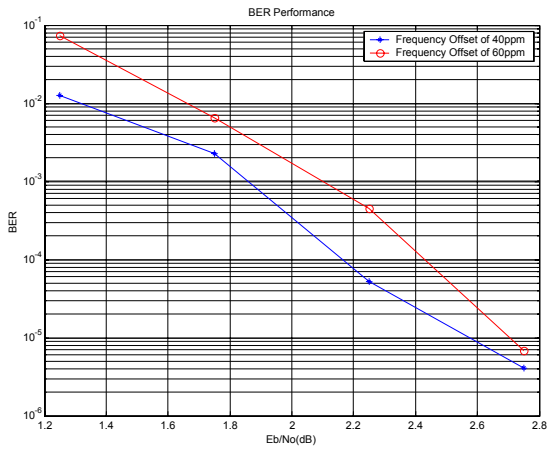


Fig. 8. BER Performance with Large Frequency Offset

V. FPGA EVALUATION

Prototype system of the proposed DSRC IVC D-IF circuit has been built using Xilinx's Virtex 4 FPGA. The measurement and test results of BER are quite close to the simulation results. The difference between simulation results and measurement results is only 0.2-0.5dB

VI. CONCLUSIOINS

A digital intermediate frequency receiver based on bandpass sampling is proposed for inter-vehicle communications. By carefully selecting the sampling rate and equivalent digital IF frequency, a simplified DDC can be employed. Moreover, with this simplified DDC, the combination of DDC and LPF is possible to reduce the complexity further. UW correlation is used for both initial frequency offset estimation and UW detection. This data aided frequency offset estimation and correction algorithm is quite robust and is able to handle very large frequency offset (up to 60ppm or 348 kHz). Therefore, the pre-compensation for the fixed frequency offset in the DDC is not necessary. To combat multipath fading, a Turbo decoder is introduced. The coding gain is about 11dB for the BER of 10^{-5}. This coding gain shall be enough to offset the degradation caused by multipath fading, as the typical multipath fading in the IVC channels is Rician fading with large Rician factor. The design has been verified by FPGA implementation and evaluation.

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