# A 3 CHANNEL DIGITAL CVSD BIT-RATE CONVERSION SYSTEM USING A GENERAL PURPOSE DSP

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## ABSTRACT

This paper presents a bit-rate conversion system for an efficient communication between two CVSD systems with different bit-rates. To ensure the robustness to external noises, the presented system is implemented in digital domain using a general purpose digital signal processor (DSP). In order to overcome the problems caused by different bit-rate and time-constants, several methods are considered in this study. In addition, a significant simplification of the system complexity is obtained by introducing the IIR filter to the decimation/interpolation process. The use of the IIR filter provides comptational advantages over the conversion system employing FIR filters, because the linear phase is not a critical issue in this application. By modifying the algorithm based on the IIR filter, a 3-channel full-duplex conversion algorithm was successfully implemented on a single DSP. Experimentals results are presented to exihibit the consistent and reliable performance of the bit-rate conversion system.

## 1. INTRODUCTION

Digital compression techniques are generally used to increase channel capacity of the telecommunication system. In spite of low compression ratio, waveform coding schemes such as log-PCM, delta modulation (DM), adaptive DM (ADM), adaptive differencial PCM (ADPCM) [1] have been widely used in communication areas mainly due to their simplicity. As one kind of the ADM coding, the continuously variable slope delta modulation (CVSD) [1-3] is a common characteristic method, which adjusts the step size based on the most recent 3 or 4 DM bits. Main advantage of the CVSD is its comparable quality to the log-PCM operating at 40 kbps and reasonable performance at the channel capacity as low as 16 kbps [1].

Since the CVSD system is diversified in its bit-rate, there exists a need to convert one bit-rate to another. For example, if one communication node is equipped with a 32k bps CVSD terminal while the other one is connected to a 16k bps terminal, there is no direct way to get right communication between two CVSD terminals without additional hardware. The communication line in this situation requires the bit-rate conversion system, which is often implemented using analog circuits based on CVSD encoder/decoder units. After converting the encoded CVSD signal to baseband analog signal, the signal may be encoded back for a new CVSD digital representation. This approach is implementable with serial connection of two CVSD codecs. However, this approach requires two CVSD codecs for one communication line which may raise cost and complexity problems. Moreover, the baseband signals can be easily corrupted by external noises such as thermal noise. These undesirable effects can be prevented by using the conversion system operating in digital domain.

The objective of this work is to develope a digital bit-rate conversion system for an efficient communication between two CVSD systems operating at different bit-rates. In particular, we are interested in the 16kbps-32kbps CVSD line. The conversion system presented in this paper can be characterized by the robustness to the environmental noises and the small hardware complexity compared with the analog system.

The conversion system is based on a genaral purpose DSP TMS320C30. In order to develope the system requiring the minimim amount of hardware, efforts are focused on minimizing the system complexity with the modification of the algorithm. The key idea of the algorithm modification is the use of IIR filter, rather than FIR filter, for the sampling rate conversion. Unlike other high quality speech coding systems, the linear phase is not a critical issue in the CVSD system, so that the use of IIR filter allows one to obtain a significant reduction of the computational load for the conversion system.

After the modification of the bit-rate conversion algorithm by employing the IIR filter and the optimization of the real-time program, it is shown that three channels of full-duplex CVSD bit-rate conversion system are successfully implemented by a single TMS320C30 processor. Experimental results are presented to demonstrate the performance of the bit-rate conversion system and its real-time implementation.

This paper is organized as follows. Section 2 describes digital CVSD coding. Analog and digital bit-rate conversion algoroithms are presented in Section 3. In Section 4 real-time implementation of the developed algorithm is described in detail. Experimental results are discussed in Section 5 and conclusion is made in Section 6.

## 2. DIGITAL CVSD CODING

The CVSD system [1-3] is one of the well-known ADM method which adopts a syllabically (or pitch) companded scheme. Instead of the instantaneous adaptation, it adjusts the step size "syllabically" over time intervals of 5-10 ms in typical. The number of adaptation memory is observed within a few recent samples, and the step size is changed relatively slowly, i.e., in *continuously variable slope*. CVSD is popular in the field of noisy channel applications such as mobile radio, because it forces the effect of

channel errors to die out quickly so that a good granular noise performance is expected. Fig. 1 shows the block diagram of the digital CVSD encoder/decoder.

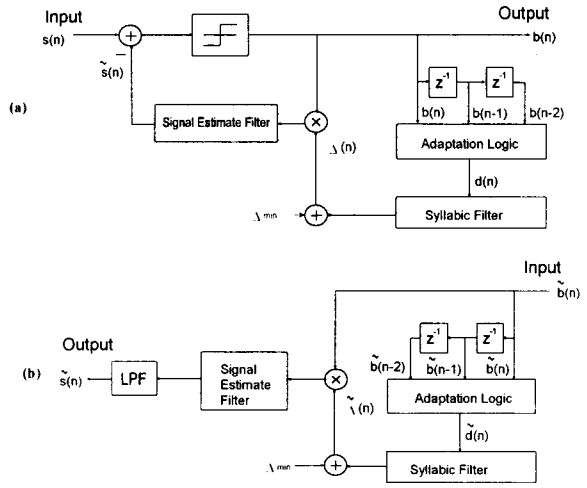


Fig. 1. Digital CVSD (a) encoder and (b) decoder.

The slope overload is detected by three consecutively identical bits in the binary sequence of the CVSD coder ouput by means of step size logic. A pulse produced by the step size logic is input to the syllabic filter. The syllabic filter produces the adaptive step size. This step size is used as the input of a leaky integrator, called the signal eatimate filter which predicts the input signal of the CVSD coder. Time-constants of syllabic and signal estimate filter should be determined as appropriate values according to bit-rate of CVSD coder.

## 3. BIT-RATE CONVERSION BETWEEN CVSD SYSTEMS

### 3.1. Analog conversion system

Interface between CVSD systems with different bit-rates can be done via a simple procedure: decoding the transmitted bit-sequence into the analog signal using a CVSD codec and then encoding it back to the target bit-rate using another codec [4]. Fig. 2(a) shows the analog conversion process for the communication between 32 and 16 kbps CVSD systems. Regardless of its simplicity in the structure, this approach has several shortcomings that need to be overcome. First of all, since the decoded signal is converted into analog domain using the D/A converter and sampling rate is modified using the A/D converter, the quantization noise cannot be avoidable during the conversion process. Secondly, this method would be more sensitive to external noises being observed in conventional analog circuits. Finally, the method requires an additional CVSD codec, which may raise cost and complexity problems.

### 3.2. Digital conversion system

By converting the bit-rate directly from the bit-stream in digital domain it is possible to avoid the problems addressed in the previous subsection. The block diagram of the digital bit-rate conversion system for the CVSD communication system is shown in Fig. 2(b) which illustrates the conversion process between 16kbps and 32knps CVSD systems. Unlike the analog approach, the input signal is decoded in the digital domain, and the sampling rate of decoded signal is converted using interpolation/decimation filters. Finally, the converted signal is encoded back in the digital CVSD format to fit for the target bit-rate. While the analog converter produces the analog signal as a baseband information, the digital converter is concerned with PCM codes as an intermediate information.

Though this approach requires a microprocessor between two CVSD codecs to implement the conversion algorithm, this system is able to avoid the quantization noise introduced by D/A and A/D processing and is robust to external noises. Despite the advantages of the digital converter, it should be mentioned that, since the conversion system comprises another decoding/encoding process, additional coding errors which are inherent from the CVSD coding itself are expected.

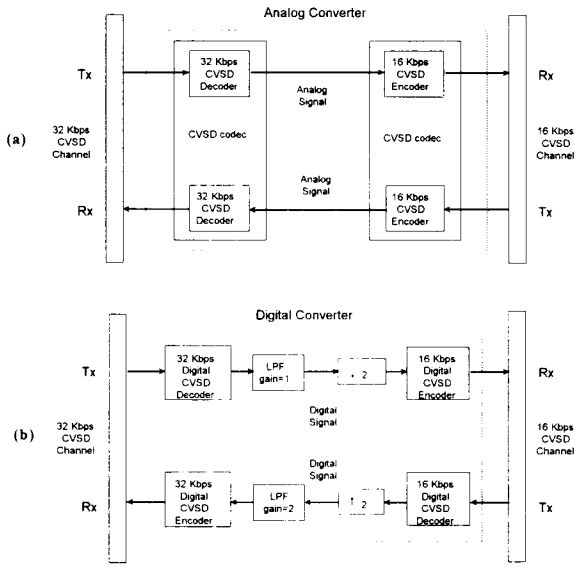


Fig. 2 (a) Analog and (b) digital conversions between CVSD systems.

### 3.3. Digital filter for sampling-rate conversion

Digital low pass filter (LPF) required for the decimation and interpolation plays an important role in determining both the overall performance as well as the complexity of the conversion system. Since baseband signal in the CVSD system is bandlimited within the range of 300 to 3400 Hz's, the digital LPF should be designed to meet the requirements that its cutoff frequency is less than 3400 Hz and the stopband attenuation is greater than or equal to 35 dB. In addition, since most of computational burden in the conversion system is brought from this filtering process, the filter must be implementable with low computational complexity while providing acceptable speech quality.

To satisfy the linear phase requirement, the finite impulse response (FIR) filter is generally employed in the interpolation and decimation process [4-6]. However, the linear phase property is not the issue of importance in

this application because, unlike other high quality speech coders, the speech quality of the CVSD coder is not seriously degraded by the nonlinearity of the phase response of the filter. More important factor to be considered is the sharp response of the filter. Considering these, the use of IIR filter will provide many advantages over the FIR filter, such as the sharp response with low computational complexity.

In this study, the elliptic IIR filter [5][6] has been chosen for the interpolation and decimation, because it exhibits equiripple behavior in both the passband and stopband and yields the smallest filter order for a given set of specifications.

The number of operations required for the decimation and interpolation are summarized in Table 1, where $N_F$ and $N_I$ denote FIR filter and IIR filter orders, respectively. Numbers in Table 1 were counted for the operations required to process one input speech sample. When $N_F = 48$ [4] and $N_I = 4$, the number of operations for the FIR and IIR filters are 96 and 35, respectively, which produces the reduction by the factor of 3.

From informal listening tests, we obseved that the use of the 4th order elliptic IIR filter does not introduce any degradation of the speech quality while reducing the system complexity significantly, compared with the case of using the 48-tap optimal FIR filter.

Table 1. Operations for interpolation/decimation using FIR and IIR filters.

| | decimation<br>32 kHz → 16 kHz | interpolation<br>16 kHz → 32 kHz |
|---|---|---|
| FIR | $N_f$ | $N_f$ |
| IIR | $3(N_I + 1)$ | $4(N_I + 1)$ |

## 4. REAL-TIME SYSTEM DESIGN

With the real-time software programmed to implement the one channel bit-rate conversion algorithm employing the IIR filter, the DSP finished the conversion by using roughly 30 % of its computational power. In the experiments, the DSP was assumed to operate with 33 MHz system clock. Based on this result, it can be said that the real-time system is able to implement the conversion for 3 channels at the maximum computational speed. To confirm this, a multichannel version of the real-time software was developed and it was experimentally shown that the 3 channel full-duplex CVSD conversion was implementable with a single TMS320C30.

The digital bit-rate conversion system for the CVSD communication system was implemented using one TMS320C30 DSP processor. By using the floating-point processor, we could avoid the scaling and overflow problems that are critical in the case of fixed-point processors.

The overall block diagram of 3 channel full-duplex digital conversion system is shown in Fig. 3. The developed real-time system consists of subscriber circuit (SC) & CVSD codec unit, interface (IF) unit and digital signal processing (DSP) unit. In the SC & CVSD unit, MX629 was used. 1.024 MHz clock is applied to MX629 chip as the reference clock and MX629 operates at the rate of 16/32 kbps depending on the applied clock rate. The IF unit constructed using the Erasible Programable Electronic Device (EPLD) consists of serial-to-parallel (S-P) and parallel-to-serial (P-S) converson section controlled by the same clock that is applied to the CVSD codec. The purpose of this unit is to provide the interface between CVSD codec and DSP units.

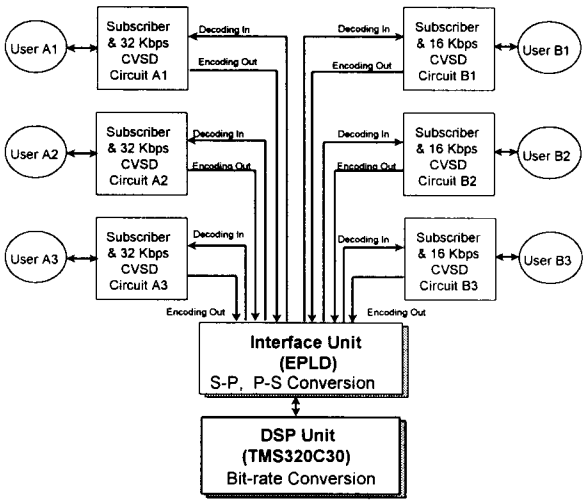


Fig. 3. The block diagram of a 3 channel digital conversion system.

The real-time conversion system is based on external interrupts synchronized with the clock of CVSD codec. Whenever interrupt is generated by the codec clock, the system I/O generates 8 bits for the 32 kbps channel, and 4 bits for the 16 kbps channel in order to synchronize both channel. The DSP unit decodes input bit-stream and converts the sampling-rate of the decoded output, and then, encodes it back to the target bit-rate. Finally, new encoded CVSD bits are sent to the IF unit. The encoding and decoding processes are executed simultaneously. Once the conversion process is completed, the system waits for a new interrupt. The flow chart of the real-time software is shown in Fig. 4.

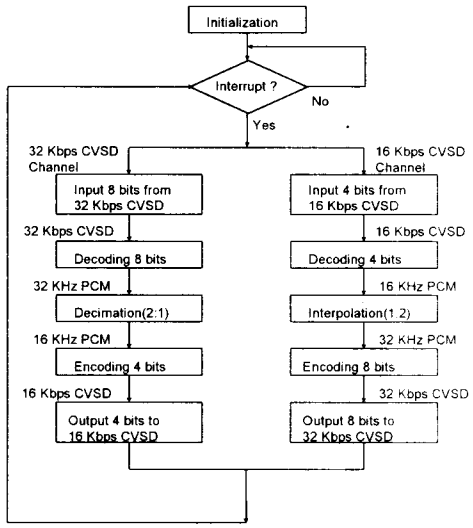


Fig. 4. Flowchart of the real-time conversion program.

The real-time software for the bit-rate conversion was implemented on the DSP. Computational complexities were measured in terms of the number of instruction clocks, and the comparison was made between the IIR-based method and the conventional FIR-based approach. The results are summarized in Table 2. We used a 4th order IIR and a 48-tap FIR filters for comparison. With 4125 instruction clocks avaiable, the real-time system implementing the IIR-based method exhibits the possibility of accomodating, at least, 3 channels in a system comprising one TMS320C30 DSP.

Table 2. Clocks for 1 channel conversion using FIR/IIR filters ( 32 kHz $\leftrightarrow$ 16 kHz).

| | conversion-FIR | conversion-IIR |
|---|---|---|
| instruction clocks | 1480 | 1098 |
| max # of channels | 2.79 | 3.76 |

## 5. EXPERIMENTAL RESULTS

In this section, experimental results are presented. Experiments were focused on verifying the effect of the time-constants of syllabic and signal estimate filters. Since the time constants are concerned with encoding/decoding process, they are very important factors in the designing the CVSD bit-rate conversion system. In general, CVSD codec uses the recommended time-constant values, but the exact values canot be obtained in case of using commercial codecs. Experiments were conducted to investigate the effects of time-constants mismatching on the quality of the synthesized speech after the bit-rate conversion.

For the case that smaller or larger time-constants is used for decoding process than those of transmission part, results are presented in Fig. 5. From the results, it can be observed that degradations due to the use of different time-constants are not significant in the conversion system.

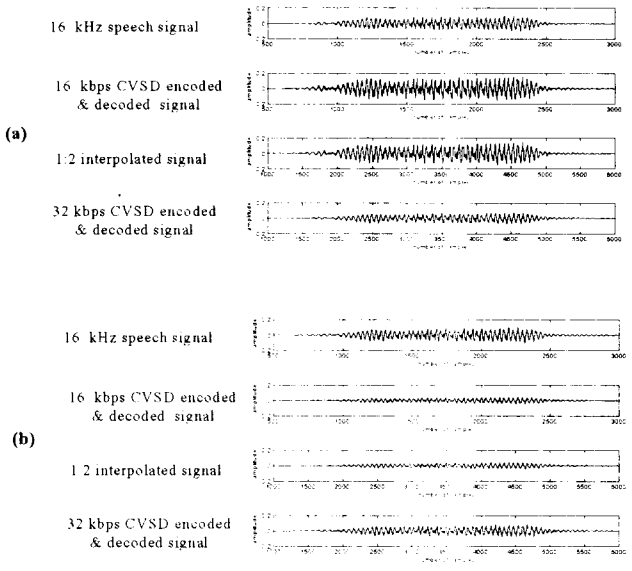


Fig. 5. Conversions with (a) smaller and (b) larger time-constants (16 kbps CVSD $\rightarrow$ 32 kbps CVSD).

Experimental results also showed that there was no noticeable difference between 16 kbps to 32 kbps and 32 kbps to 16 kbps cases. Similar results were obtained for the case that larger time-constants are used for decoding than those of CVSD codecs in the transmission part.

The developed system was compared with the conventional system under normal on-line conditions. The proposed system showed the performance better than or equal to the conventional one in terms of the SNR summarized in Table 3. In addition, it should be noted that the new system would outperform the conventional one under the adverse conditions such as high or cold temparature.

Table 3. SNR performances of analog and digital converters (32 kbps CVSD $\rightarrow$ 16 kbps CVSD). reference signal: -15 dBmo, 800 Hz sinewave

| level (dBmo) | spec. (dB) | analog (dB) | digital (dB) |
|---|---|---|---|
| -15 | 10 | 15 | 15 |
| -10 | 10 | 15 | 15 |
| -5 | 10 | 15 | 15 |
| -0 | 10 | 15 | 16 |

## 6. CONCLUSION

A bit-rate conversion system for the CVSD communication system has been presented. The conversion algorithm has also been implemented using a general purpose DSP processor. Since the system operates in the digital domain, it overcomes the problems often encountere in the analog system. such as quantization noises and external noise corruption. To reduce the computational complexity, the IIR filter is employed for the interpolation/decimation. By using the IIR filter and optimizing the real-time program. 3 channel full-duplex conversion system was successfully implemented on a single DSP processor. Experimental results showed that the use of IIR filter provided several advantages in system complexity and the real time system exihibited a reliable and consistent performance even when there exists the time-constant mismatch.

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