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DEVELOPMENT OF A FLASH MEMORY DRIVE FOR ATA BUS

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Abstract

In this treatise, we have designed and constructed a flash memory drive using the ATA bus method for flash memories, which is an element of semiconductors, in order to improve the problems with existing hard disks.

Common hard disks are sensitive to impact or shock and because of this, errors in the data or disks occur. Also, due to its internal structure, it requires much electricity and is not suitable to make it light-weight. However, by using flash memory, which is an element of semiconductors, to produce hard disks, low electricity start up becomes possible, not to mention light-weight. It is also strong against external impact and is expected to be utilized for embedded systems, black boxes, vehicles, ships, as well as for other industrial and military use.

INTRODUCTION

Currently, the most commonly used additional memory devices for PCs and servers are hard disks which use a disk revolution method. With the recent sales of S-ATA hard disks, high-capacity hard disks have now become available at a reasonable price. However, a disadvantage with this these hard disks is that in order to access data, a spindle motor rotates rapidly, thus costing high electric power. Also, the physical structure of this is that the semiconductor head rises about 0.1㎛ above the disk surface in order to read and write data. This structure makes it prone to colliding with the disk surface when impacted or power is suddenly turned off, making it possible for the inability to read or store data.

Therefore this treatise deals with the design, production and evaluation of a hard disk using flash memory in order to solve the problems with common hard disks.

MAIN SUBJECT

The common hard disks that we use uses a disk rotation method as shown below in picture 1 and is composed of a spindle motor that rotates the disk, disk to store the data, and a head to read and write data. The spindle motor is particularly important because it decides the data handling speed of the hard disk's spindle motor speed and head access time.

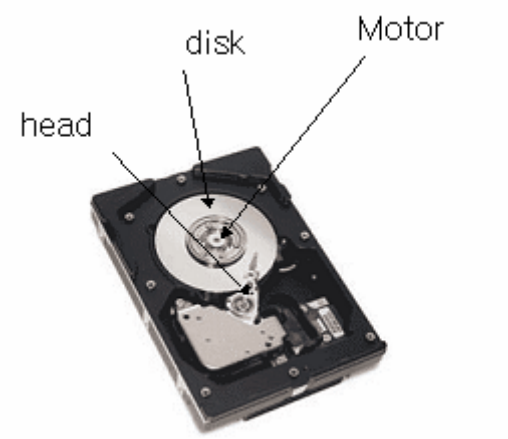

Figure 1. Structure of common hard disks

Today's reality is that IDE hard disks using a motor start-up method at 15,000 rpm is the standard in sales. However, with the increase in speed, it commonly becomes more sensitive to impact and mechanical supplements to prevent impact are being developed in various ways. Lately, however, additional memory devices for car PCs and embedded systems use flash memory, and there is a trend to utilize it in more ways as well. Due to this timely necessity, SCSI and ATA method flash memory disks are being sold overseas, but it is developed nowhere domestically.

Domestically, USB memory sticks are an additional memory device which uses flash memory that is being used widely, however, it is not possible yet to use as a booting disk for PCs.

Therefore, in this treatise, we have designed and produced a hard disk that uses flash memory as a booting disk for personal computers.

HARDWARE DESIGN

In order to design and produce the additional memory device through flash memory for personal computers, we have used the basic structure of the ATA interface to design the hard disk.

Since most common PCs use ATA hard disks to boot their OS, we have placed our

objective in realizing an IDE flash disk as shown in picture 2.

Most ATA interfaces support both 8 bit and 16 bit. However, for the sake of simplicity of the system in this treatise, we have designed the interface. [1]

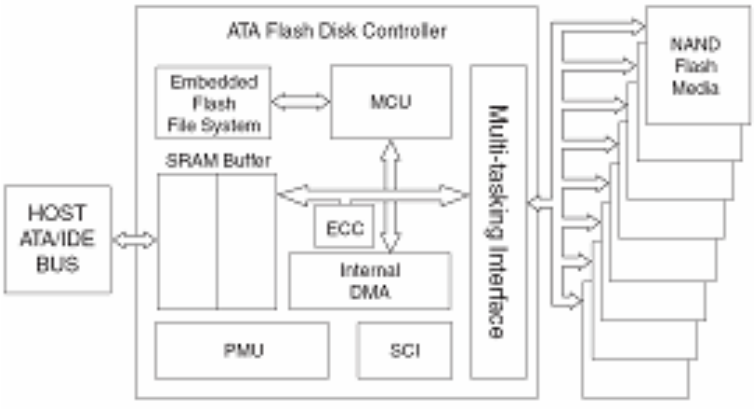

Figure 2. Hardware of Flash Memory Disks

Finally, in order to embody the most suitable control and high-speed data processing for each part, we have used the TMS320C33 for the MCU.

Also, in order to solve the problem with the bottleneck effect of the data while the data is being handled between the PC and hard disk, we have added an SRAM buffer. And in order for the efficient address management of the attached flash memory, we have embodied a DMA.

Also, in order to produce flash memory disks of various capacities, we have used single layer flash ROMs K9F1208, K9F1G08, and K9F4G08 and dual layer flash ROM K9W8G08 from Samsung semiconductors.

Figure 3. ATA Flash Drive hardware produced

EMBEDDED WEAR-LEVELING ALGORITHM

For the commonly used NAND Flash Memory, its transmission speed for storing high volume data is faster than NOR Flash Memory, and is relatively cheaper. Structurally, however, it has problems that the cell's life expires if there are more than 300,000 data on one page. In order to solve this problem, we used wear-leveling algorism in this treatise.

Normal wear-leveling algorism changes the absolute address of the memory, which is delivered from the DMA, to the relative address in order to solve the problem with shortened cell life by repeatedly storing the addresses.

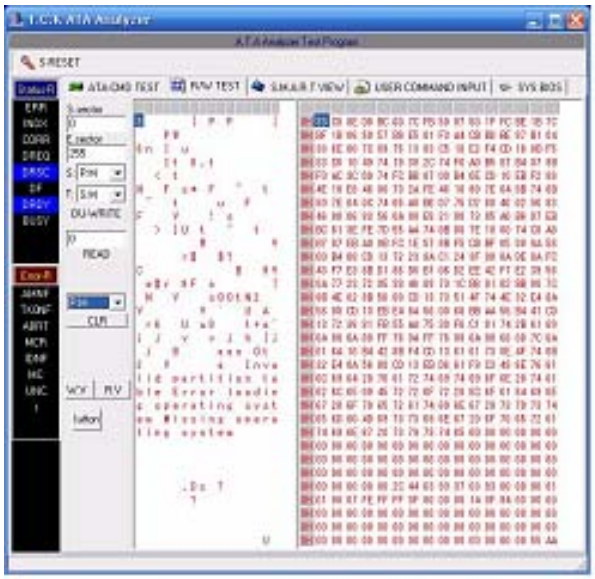

Figure 4. wear-leveling Test Program

For most OS, the FAT is directly administered by the OS and the FAT structure constantly changes. Accordingly, if there 100,000 changes a day in the FAT, 3 days later, the FAT pages stored in the flash memory dies, making the hard disk unusable. Therefore, when designing a flash disk, the flash memory life must be improved through wear-leveling algorism.

Wear-leveling algorisms from M-systems were used to create the system in this treatise. Picture 4 is a program made by using visual c++ in order to test the algorism. The test method was to save data on sector 1 and then reread the data. The results were that there were no problems after 5,000,000 plus actions.

FIRMWARE DESIGN

For the hard disk using flash memory as proposed in this treatise, the ATA bus interface is linked to the PC and structure is made up of a flash memory that uses the existing ATA physical disk and head. In order to process the ATA commands, there is

an interface processor. In order to analyze this command, it is composed of a microprocessor interface and DMA interface, buffer memory, decoder that can choose each flash memory, boot memory, flash memory bank, and a part which can select the host adopter interface and mode.

This structure is a change from the existing ATA physical structure to a flash memory structure. This greatly improves problems with the additional memory device of the physical structure and has the disk structure which has the possibility to develop into lower electricity and smaller sizes. In order to operate from a disk using this structure, it is important to develop suitable firmware, and firmware is particularly needed to process the read and write commands in order to satisfy the structural specifics of flash memory.

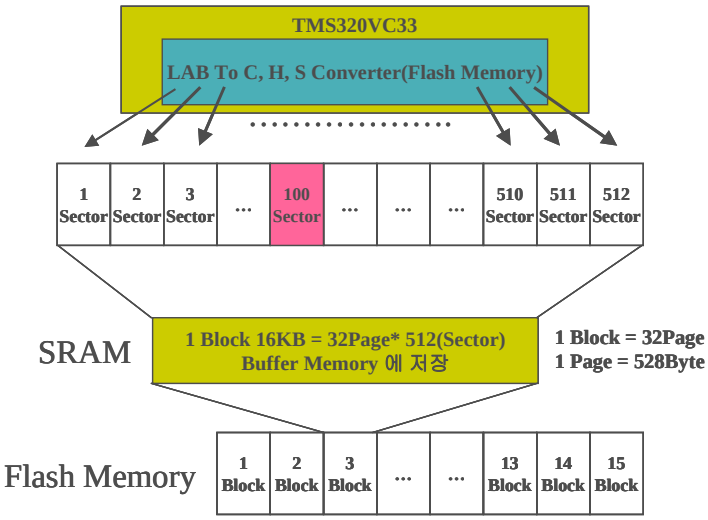

Figure 5. ATA read/write using Flash Memory

CONCLUSION

From this research, we can expect acquirement of key technology of the ATA Flash Memory Drive, and through intellectual rights gained from the design of the ATA Flash Memory Drive, we have secured company competitiveness. Also, the ATA Flash Memory Drive developed in this research is expected to be utilized in various embedded systems and especially from 2007, when cars will be required to attach it as a recording device, the demand for it is expected to rise. In the future, we are planning to develop it for 2.5 inch laptops and slim-types.

Chart 1. Comparison of normal HDD and Flash Memory Drive

Evaluated Item	HDD	F.M.D
Compatability	100%	100%
Transmission Speed	20MB/S	10MB/S

Electricity	550mA, 5VDC	150mA 5VDC
Durability	1,000,000 Cycle	5,000,000 Cycle
Life	87,600 hrs	87,600 hrs
Temperature	−45C~ 85C	−45C~ 85C
Humidity	5% ~ 95%	5% ~ 95%

Figure 6. Flash Memory Drive for ATA bus

REFERENCES

[1] The Scsi Bus and IDE Interface, Addison-Wesley Pub Co, "*Schmidt, Friedhelm/ Shultz, J.Michael (Tr)*", 1995.4
[2] *TMS320C33 User's Guide*, Texas Instruments, 2004. 4.

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