# SUBBAND DIGITAL PREDISTORSION BASED ON INDIRECT LEARNING ARCHITECTURE

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# ABSTRACT

This paper deals with the linearization of RF power amplifiers (PAs) using digital predistortion (DPD) technique. One of the most important constraint on DPD implementation is digitization of PA output signal needed for identification of predistorter model. The bandwidth of this signal may be 3 to 7 times wider than the bandwidth of the input signal. The sampling rate required for accurate compensation of out-of-band distortions is thus very high, and has a direct impact on power consumption and implementation complexity of DPD identification algorithms on digital processor. In this paper, we propose a new iterative DPD identification algorithm based on the Indirect Learning Architecture (ILA) and on subband decomposition of PA output signal. The proposed algorithm converges to conventional ILA solution with a drastic decrease in required sampling rate.

*Index Terms*— Subband Decomposition, Digital predistorter, Power Amplifiers, Indirect Learning Architecture, Linearization.

### 1. INTRODUCTION

PAs usually exhibit nonlinear characteristics when driven towards high efficiency saturation region, which cause spectral regrowth beyond the signal bandwidth [1]. Waveforms having high peak to average power ratio (PAPR) such as CDMA of OFDM make necessary the linearization of PA to improve its power efficiency [2, 3].

Digital predistortion (DPD) based on Indirect Learning Approach stands out as one of the most popular techniques to linearize PAs [4]. A PA preceded by a predistorter can be driven more towards the high efficiency saturation region with less nonlinearity effects [2].

In order to extract the predistorter model, PA output signal is first translated to an Intermediate Frequency (IF) or to baseband (Zero IF) and then digitized using an AtoD converter. The required sampling rate for an accurate representation and thus compensation of  $n^{th}$  order intermodulation products is equal to n.BW, where BW is the RF bandwidth of the input signal. Complexity, power consumption and requirements related to signal digitization and implementation of predistorter identification algorithm depend primarily on the sampling rate. DPD accuracy in conventional ILA is expected to improve as the sampling rate is increased.

Predistorter architecture allowing to reduce sampling rate while taking into account high order intermodulation products has been seldom addressed in the literature. In [5] the authors propose an architecture based on direct learning (DLA) which allows to undersample the output of the PA, but this approach is dedicated to a specific predistorter architecture. It has been demonstrated that undersampling the output of the PA is not a problem for direct identification [6] and thus for DLA, while it remains an issue for ILA which in turn exhibits a lower computational complexity than DLA [7]. Subband predistortion approaches have also been proposed, [8–10], to apply different predistorsion functions depending on the subband using either ILA or DLA. But the proposed schemes do not allow to reduce the sampling frequency of the signal at the output of the PA.

In this paper we propose an original approach to decompose PA output signal into smaller bandwidth signals and digitize each signal individually with a possibly lower sampling rate. We propose a new iterative predistorter identification algorithm based on the ILA architecture and on subband decomposition of the PA output signal. It will be shown that this algorithm converges to the conventional ILA solution with a convergence time which depends on the amount of information about PA out-of-band emissions.

The remainder of this paper is organized as follows : First, after recalling the conventional ILA identification approach, we present the new DPD structure based on subband decomposition. In Section 3, we will built arguments on the convergence properties of the proposed algorithm through step-by-step system transformations. Finally, we present simulation results in Section 4, followed by a discussion and conclusion section.

# 2. PRINCIPLE OF THE SUBBAND PREDISTORTER

#### 2.1. Regular Postdistorter Architecture

A conventional baseband model of ILA is shown in Fig. 1. The post-inverse model of PA is first identified and then used as a predistorter in front of the PA. The main goal is to identify a set of parameters for the post-distorter block in order to render the overall system made of the predistorter and PA linear. The training procedure is required to be repeated several times until the error e(n) is minimized. If the postdistorter model is conveniently chosen this algorithm converges and the energy of the error  $||e(n)||^2$  becomes negligible [11].



Fig. 1. Indirect Learning Architecture

If the post-inverse is modeled as a Memory Polynomial, then its output can be written as:

$$z_p(n) = F(z) = \sum_{k \in K} \sum_{l \in L} c_{kl} z(n-l) |z(n-l)|^k, \quad (1)$$

where F(z) is the nonlinear function of the postdistorter which is, for MP model, the sum of the nonlinear terms of the form  $z(n-l)|z(n-l)|^k = z^{k/2+1}(n-l)z^{*k/2}(n-l)$ . The sets K and L define the nonlinearities and the memory of this model. Equation (1) can be rewritten in matrix form:

$$\underline{\mathbf{z}}_p = \underline{\underline{\mathbf{Z}}} \, \underline{\mathbf{c}}.\tag{2}$$

The least Square solution for  $\underline{\mathbf{c}}$  which minimizes  $||e(n)||^2$  is:

$$\hat{\underline{\mathbf{c}}} = \left(\underline{\underline{\mathbf{Z}}}^H \underline{\underline{\mathbf{Z}}}\right)^{-1} \underline{\underline{\mathbf{Z}}}^H \underline{\mathbf{z}}_p.$$
(3)

Identification of  $\hat{\mathbf{c}}$  is always an iterative process whatever is the method used to solve (3) [7]. Each iteration, named "system" level iteration, allows the system which is formed by the tandem connection of the predistorter and the PA to converge towards a linear system. This happens when the error e(n)becomes ideally null, which means that  $z_p(n) = x(n)$  and thus y(n)/g = u(n), since P = P', where g is the linear gain of the PA.

# 2.2. Subband Postdistorter Architecture

In this section we present an intuitive explanation of the subband predistorter architecture. In the conventional ILA DPD system depicted in Fig. 1, we have the equality u(n) = z(n)



(a) Equivalent ILA architecture after convergence



(b) Subband architecture for ILA DPD

Fig. 2. Subband DPD

after convergence for a given postditorter model. Thus the input to the postdistorter z(n) has no energy outside the band B of the input signal u(n), with the following definition:

$$U(f) \neq 0$$
 if  $|f| \leq B$  and  $U(f) = 0$  otherwise. (4)

So after convergence Fig. 2a is equivalent to Fig. 1, where  $H_{CH}$  and  $H_{IM}$  are ideal brick wall filters with zero phase. Their bandwidth definitions are given by:

$$|H_{CH}| = \begin{cases} 1 & \text{if } |f| \le B, \\ 0 & \text{else.} \end{cases} \quad |H_{IM}| = \begin{cases} 1 & \text{if } |f| > B, \\ 0 & \text{else.} \end{cases}$$

The filters  $H_{CH}$  and  $H_{IM}$  are represented in the predistorter (Fig.2a) for the sake of symmetry with the post-distorter and to mimic the reference block diagram sketched Fig. 1. But from (4) and (5)  $H_{CH}$  and  $H_{IM}$  are obviously useless in the predistorter.

It is seen from Fig. 2a, that the error e(n) can be expressed as:

$$e(n) = x(n) - z'_p(n) = (x(n) - z_{IM}(n)) - z_p(n),$$
 (6)

which corresponds to the block diagram depicted Fig. 2b. It is worth noting that  $H_{IM}$  could be split into a uniform filter bank where each filter will be passband filter with bandwidth equal to B as shown in Fig. 3:

$$|H_{IM_p}| = \begin{cases} 1 & \text{if } (p-2)B < |f| \le pB, \\ 0 & \text{else.} \end{cases}$$
(7)



Fig. 3. IM Filter bank

# 3. DISCUSSION ON THE SYSTEM CONVERGENCE BEHAVIOR

In this section we will provide some means to have a better understanding about system convergence of the proposed identification architecture. The postdistorter model that will be used for this rationale is a memory polynomial (MP) model (1).

From the previous section we can see that the proposed identification algorithm behaves asymptotically as the regular one. Indeed when the system has converged we have y(n) = g u(n) and then, there is no energy outside B at the input of the postdistorter (4). Thus Fig. 2a can be seen as equivalent to Fig. 1. But going from Fig. 1 to Fig. 2a involves modification of the postdistorter model (1).



Fig. 4. Transformations of the Postdistorter Architecture

In the sequel of this section we will detail this modification, that will be split into different steps. For the sake of simplicity, but without loss of generality, we will consider the postdistorter model sketched in Fig. 2b with only the  $H_{CH}$ and  $H_{IM_3}$  bands. If the filters are ideal and defined in (5) and (7), then  $z(n) = z_{CH}(n) + z_{IM_3}(n)$  and (1) can be rewritten as (Fig. 4b):

$$z_p(n) = F(z_{CH}) + F(z_{IM_3}) + C(z_{CH}, z_{IM_3})$$
(8)

where  $C(z_{CH}, z_{IM_3})$  is the sum of nonlinear cross terms of the form  $z_{CH}^{k_1}(n-l)z_{IM_3}^{k_2}(n-l)z_{CH}^{*k'_1}(n-l)z_{IM_3}^{*k'_2}(n-l)$  with  $k_1 + k_2 = k/2 + 1, k'_1 + k'_2 = k/2$  and  $k_i, k'_i > 0$ . The second transformation step (Fig. 4c) restricts the postdistorter model to the following equation:

$$z_p(n) = F(z_{CH}) + F(z_{IM_3})$$
(9)

thus neglecting the cross terms in (8). This obviously reduces the amount of information used for the computation of  $\underline{\hat{c}}$  (3). Finally, the last transformation step of the postdistorter model (Fig. 4d) corresponds to the following equation:

$$z_p(n) = F(z_{CH}) + z_{IM_3}(n).$$
(10)

This transformation scales  $z_{IM_3}(n)$  and discards the delayed versions and nonlinear terms of  $z_{IM_3}(n)$ . Which is again a loss of information.

The main thing is that when  $z_{IM_3}(n) = 0$ , *i.e.* when the ILA architecture has converged, (10) is equivalent to (8). This highlights that the regular architecture and the one proposed in this paper are asymptotically the same. Fig. 5 shows the convergence of the algorithm through the Normalized Mean Square Error (NMSE) for the four postdistorters sketched in Fig. 4. For these simulations, the filters are equiripple FIR filters (more details are given in the next section) and we can see that the imperfections of this filter bank gives rise to a loss of information (difference between ILA and Arch 1 curves) that should not occur with perfect ideal brick wall filters. We can see that, after some system iterations (4 in this example), Arch 1, Arch 2 curves are very close and that the loss of information coming from the modification between Arch 1 and Arch 2 impacts mainly the convergence speed but does not bias the result. We can also check that the Sb curve follows closely the Arch 2 one. We can conclude by saying that these simulation results confirm the asymptotic behavior of the subband postdistorter architecture that was inferred in this section.



**Fig. 5**. NMSE *vs* system iterations for the four postdistorter architectures: *ILA* (Fig. 4a), *Arch 1* (Fig. 4b), *Arch 2* (Fig. 4c) and *Sb* (Fig. 4d)

#### 4. SIMULATION RESULTS AND DISCUSSION

The proposed subband DPD architecture has been evaluated through baseband Matlab simulations. We present here



**Fig. 6**. Figures of merit *vs* postdistorter identification architecture: *ILA* (Fig. 4a), *Arch 1* (Fig. 4b), *Arch 2* (Fig. 4c) and *Sb* (Fig. 4d)

the results obtained with a PA modeled by a Wiener model proposed in [12]. The waveform is an LTE signal having a bandwidth of BW=20 MHz with a PAPR of approximately 11 dB. The sampling frequency is 122.88 MHz. Three filters are used in the post-distorter path (Fig. 2b and 3):  $H_{CH}$ ,  $H_{IM_3}$  and  $H_{IM_5}$ . As the simulation is baseband  $H_{CH}$  is a low-pass filter with (BW/2) MHz bandwidth and all other filters are pass-band with bandwidth equal to  $K \cdot BW$  MHz and center frequencies respectively equal to  $K \cdot BW$  MHz,  $2 \cdot K \cdot BW$  MHz and  $3 \cdot K \cdot BW$  MHz, with  $K \leq 1$ .

The results presented in Fig. 6 have been obtained using Equiripple FIR filters with K = 0.9 and a transition band-

width of 500 KHz. The three different figures of merit for a predistortion system which are presented are the spectrum at the output of the PA, the Error Vector Magnitude (EVM) and the lower Adjacent Channel Power ratio (ACPR). After the four kinds of postdistorter have converged, *i.e.* system iteration 10 in this simulation, we can see that the output spectra reach approximately the same level of performance, Fig. 6a. This shows again that postdistorter architectures Fig. 4a and 4d behave the same after some system iterations. Even if Fig. 6c shows a slow-down of the convergence with the transformation of the postdistorter from *ILA* to *Arch 1* and even more from *Arch 1* to *Arch 2*, the biggest impact on the convergence speed appears to be for the ACPR, more precisely with the modification from *Arch 1* to *Arch 2* which impacts significantly the decreasing of the ACPR vs system iterations.

Fig. 7 shows the convergence rate concerning the decrease of the upper ACPR. The different results are obtained by varying the bandwidth parameter K of the  $H_{IM_x}$  filters applied on the intermodulation products bands (Fig. 3). It can seen that the algorithm shows a converging behavior even with very few informations on intermodulation products (K = 0.2) and that the convergence rate has a low sensitivity to K for  $K \ge 0.8$ .



Fig. 7. ACPR performance vs adjacent filters bandwidth

## 5. CONCLUSION

We have proposed in this paper a new ILA DPD architecture based on subband decomposition of the output signal of the PA. It has been shown that the proposed architecture corresponds to a modification of the postdistorter model that may impact the convergence rate, but has an asymptotic behavior similar to the regular ILA DPD architecture. The sensivity to the effective bandwidth of the feedback filters has also been discussed. This new architecture allows to relax the AtoD converter requirements: sampling frequency, dynamic range and thus power consumption. This also gives the possibility to decrease the complexity (Number of operation per second) of the identification algorithm.

### 6. REFERENCES

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