# AUSTRALIAN SKA PATHFINDER: DIGITAL SIGNAL PROCESSING IMPLEMENTATION AND EARLY ENGINEERING TEST ARRAY RESULTS

J. Tuthill, T. Bateman, A. Brown, J. D. Bunton, G. Hampson, A. Hotan, S. Neuhold, J. Reynolds, T. Shimwell and M. Voronkov

CSIRO Astronomy and Space Science, Australia

#### ABSTRACT

The Boolardy Engineering Test Array (BETA) is the first prototype of the Australian Square Kilometer Array Pathfinder (ASKAP), a new radio telescope that is pioneering the use of Phased Array Feed (PAF) technology in radio astronomy to provide instantaneous wide field-ofview imaging. BETA consists of six 12 meter parabolic antennas, each equipped with a 188-element PAF at the focus and a signal processing system capable of imaging an instantaneous 7 square degree field-of-view with a bandwidth of 300MHz at a resolution of 18kHz. In this paper we describe the architecture of the digital signal processing chain and its implementation on reconfigurable hardware based on Field-Programmable Gate Array (FPGA) technology. We present early engineering results taken by the instrument during commissioning trials at the Murchison Radio Observatory (MRO) in remote Western Australia. In particular, we present the first multi-beam image of an astronomical source captured with a PAFbased interferometer.

*Index Terms*— Phased arrays, Field programmable gate arrays, Channel bank filters, Array signal processing, Radio astronomy

#### **1. INTRODUCTION**

The Australian Square Kilometer Array Pathfinder (ASKAP) is the first of a new type of synthesis imaging radio telescope which employs Phased Array Feeds (PAFs) to provide an instantaneous wide field-of-view and unprecedented survey speeds [1]. The Boolardy Engineering Test Array (BETA) is the first working prototype of ASKAP and consists of a 6-antenna sub-array of the full 36-antenna ASKAP instrument [1].

Synthesis imaging radio telescopes produce a map of the intensity distribution,  $I_f(l,m)$ , of celestial sources from the complex-valued mutual coherence function,  $V_f(u,v)$ , measured by the array (termed *visibility function* for a delay compensated array). Under reasonable assumptions for most radio astronomy conditions and for small angular resolutions, the intensity distribution and visibility functions are related by the 2D Fourier transform [3] as follows

$$V_f(u,v) \cong \iint I_f(l,m) e^{-j2\pi f(ul+vm)}.dldm$$
(1)

where (u, v) are the coordinates of a reference plane perpendicular to the line of sight and measured in units of wavelengths of the centre frequency of the signal band, f. The coordinates (l,m) are the source positions on the sky projected from the celestial sphere onto a flat reference plane [4].

For the BETA phased array fed antenna, the visibility function in (1) is computed in digital hardware from the cross-correlation of beam voltages as follows

$$V_{f,i,j,k} = \sum_{j,k} B_{f,j,k} (nT + \tau_{ij,k}) B^*_{f,j,k} (nT), k = 1, 2, \dots, K$$
(2)

where  $B_{f,i,k}(nT)$  is the beam voltage for the *i*th antenna and *k*th beam and  $\tau_{ij,k}$  is the propagation path length delay difference between antennas *i* and *j*, for the *k*th beam and referenced to the (u, v) plane. *T* is the sample period. The *K* individual beams are generated by phasing together two or more of the 188 PAF element signals. In this way multiple beams can be generated concurrently to cover large angular regions of the sky simultaneously.

In this paper we describe the BETA digital signal processing (DSP) system that generates the raw beamformed visibilities,  $V_{f,i,j,k}$ , in (2) for 18 beams and 16,416 narrow frequency bands across the 300MHz total bandwidth of the instrument. Narrowband processing permits concurrent spectral line and wideband continuum observing while also allowing any channels containing high radio frequency interference (RFI) to be excised [4].

In the next section we present the DSP architecture of the BETA instrument. In Section 3 we describe the implementation of the DSP system in FPGA hardware and in Section 4 we present early measurement results taken during recent commissioning trials; including the first multibeam image of an astronomical source captured with a PAFbased interferometer.

#### 2. BETA SYSTEM ARCHITECTURE

The BETA and ASKAP DSP architectures are founded on the FX correlator structure [5][6][7] where the analysis into



Figure 1. BETA system digital signal processing architecture.

narrow frequency bands (F) is done prior the crosscorrelation computation (X) that generates the final visibilities. However, BETA and ASKAP diverge from the conventional *FX* structure in that the *F* is done in two stages and a mid-stage beamformer is implemented between those two stages. (Following the nomenclature for correlators in radio astronomy, BETA and ASKAP would be an *FBFX* correlator.)

An overview showing two of the six identical DSP paths of the BETA 6-station interferometer system is given in Figure 1. In each path, 384 MHz of RF signal bandwidth from each of the 188 PAF elements is down converted to the second Nyquist zone of the analogue-to-digital converters (ADCs) (operated at 768MSamp/s). The sampled PAF data is processed through two filterbank stages. The first *coarse* filterbank (CFB) stage channelizes the signals into 384 coarse 1MHz channels of which only the centre 304 are retained for further processing. The second *fine* filterbank (FFB) stage further divides the 1MHz channels into 54 x 18.52kHz sub-bands giving a total of 16,416 fine channels at 18.52kHz resolution.

A key advantage of partitioning the frequency channelizer into two stages is that the PAF beamformer can be most efficiently implemented mid-stage as 304 separate narrow-band beamformers, each operating on a separate 1MHz coarse frequency channel (and hence at a much lower sample rate than at the raw PAF data rate of 768 MSamp/s). Since the second-stage fine filterbank is operating on beam data rather than raw PAF element data, a reduction in the filterbank data throughput rate by a factor of approximately 10 is achieved (188 PAF-elements/18-beams  $\approx 10$ ).

The 16,416 fine channels for 18 beams from each of the six antennas are transported to the correlator where the visibilities for down-stream imaging are computed. To

provide the capacity for polarimetry [4], the correlator operates on beam-pairs from each antenna path where it is assumed that each pair contains X- and Y-polarization data for the same beam look direction (the PAF elements are arranged with 94 elements in the X-polarisation and 94 elements in the Y-polarisation). The correlator computes the cross-correlations between all 6 antennas beams for both polarization resulting in  $(2 \times 6 + 1) \cdot (2 \times 6)/2 = 78$  products for each of the 9 beam pairs and 16,416 fine frequency channels. The total correlator output in one integration period is therefore

# 78×9×16,416 = 11,524,032

complex-valued visibilities. The visibility data produced by the correlator are transported to a high-performance computing centre for final imaging processing. In the following section we describe the implementation of the DSP functions shown shaded in Figure 1. The imaging operations following the correlator are not discussed in this paper.

#### **3. IMPLEMENTATION**

The DSP for BETA is carried out on two custom-made, FPGA-based hardware platforms: the *Dragonfly-2* and the *Redback-2*. The Dragonfly-2 provides the DSP functionality for the pedestal electronics end of the processing chain (see Figure 1), including sampling and the first stage coarse filterbank (CFB).

	Dragonfly-2	Redback-2	Total FPGAs
CFB	288 cards	-	288
Beamformer	-	96 cards	384
Correlator	-	32 cards	128

Table 1. DSP hardware platform and FPGA quantities for the BETA implementation.

The Redback-2 is designed to be software reconfigurable so that the same hardware platform can be

used for the beamformer and second-stage filterbank as well as for the correlator. A summary of the hardware platform quantities for the BETA system is provided in Table 1.

#### 3.1. Coarse Filterbank

A block diagram of the polyphase coarse filterbank (CFB) is shown in Figure 2. For hardware efficiency the CFB is operated in "dual-real" mode [8] and accepts two real-valued ADC input signals and produces output busses that contain coarse channels for both ADC input ports.



Figure 2. CFB unit structure for 2 PAF elements. (2R = 2 lanes) of real-valued data, 3C = 3 lanes of complex-valued data)

The prototype channel filter for the CFB is a 12,228 tap linear-phase FIR filter (768 polyphases x 16 taps). The transfer characteristic is a constrained equiripple response designed using the Parkes-McClellan algorithm [9].

The CFB is operated in overlapped block-mode [10] with an overlap factor 40 samples in 256, resulting in a fractional oversampling ratio of 32/27. The prototype filter response coupled with the oversampling ratio deliver a passband ripple of 0.2dB across all subbands in the processed bandwidth and an image rejection of better than 62dB.

The CFB for each PAF is implemented on 48 Dragonfly-2 cards (48 Xilinx Virtex-6 XCVLX130T FPGAs). (Each FPGA contains two instances of the CFB in Figure 2.) An FPGA implementation summary of the CFB is provided in Table 2.

DSP clock rates (MHz)	256, 303, 384
FPGA registers/LUTs	35%/40%
FPGA block RAM	60%
FPGA 48-bit multipliers	70%

Table 2. FPGA implementation summary for the CFB.

#### 3.2. ACM, Beamformer and Fine Filterbank

The data arriving into the central site processing from each antenna system consists of 188 PAF elements x 304 x 1MHz channelised streams. A cross-connect routes each 1MHz channel for all 188 ports to the inputs of a beamformer (Figure 3).



Figure 3. Beamformer FPGA computational unit.

The beamformer engine in Figure 3 is a narrow-band structure [11] and is capable of producing up to 18 individual beams formed from all or a subset of the 188 PAF elements. The beamformer operates in sample-mode and produces 9 beam-pairs for each input coarse frequency sample. The complex-valued beamformer weights are updated on-the-fly by the telescope control software. The 188x188 element PAF Array Covariance Matrix (ACM) is also computed and stored in FPGA hardware as shown in Figure 3. This is a critical data product used by the telescope control software to compute the beam weights.

The fine filterbank (FFB) that follows the beamformer is a critically sampled, 64-point polyphase filter with a 12 frame front-end FIR filter. The FFB channelizes each oversampled 1MHz beam into 64 x 18.52kHz fine frequency channels. Note that due to the oversampling in the CFB, only 54 of the 64 fine channels are retained for further processing (54 x 18.52kHz = 1MHz).

Two physical instances of the FFB exist in each FPGA and are time-shared between the 9 beam-pairs output from the beamformer. Furthermore, for hardware efficiency the FFBs are operated in block mode generating 1024 samples of fine channel data for a given beam before moving on to the next beam. A data corner-turn operation is needed to ensure that contiguous blocks of 1024 samples for a given beam pair are presented to the FFB inputs. The corner-turn requires significant data storage beyond the capacity of FPGA internal block RAM and external DDR3 SDRAM is used for this purpose as shown in Figure 3.

DSP clock rates (MHz)	200, 320
FPGA registers/LUTs	40%/65%
FPGA block RAM	40%
FPGA 48-bit multipliers	70%

Table 3. FPGA implementation summary for the ACM, beamformer and fine filterbank.

The full 304MHz bandwidth ACM, beamformer and fine filterbank for each PAF is implemented on 16 Redback-2 cards with the DSP FPGA firmware configured for *beamformer-mode* operation (64 Xilinx Virtex-6 XCVLX240T FPGAs). A summary of the FPGA implementation is provided in Table 3.

### 3.3. Correlator

The correlator is operated in block mode using the same 1024-sample block length as the FFB. A complex multiply-accumulate (CMAC) and short-term accumulator memory work together to compute the 78 cross-correlation products across the 1024-sample block of the current beam pair arriving on the 6 incoming streams (Figure 4). At the end of the 1024-sample block the 78 products in the short-term accumulator are accumulated with the products for the corresponding beam pair from a long-term accumulator. The large storage requirements for the long-term products (which are the final visibilities) preclude the use of internal FPGA block RAM and are stored in external DDR3 SDRAM as shown.



Figure 4. Correlator unit structure.

The BETA correlator is implemented on 32 Redback-2 cards with the DSP FPGA firmware configured for *correlator-mode* operation (128 Xilinx Virtex-6 XCVLX240T FPGAs). A summary of the FPGA implementation is provided in Table 3.

DSP clock rates (MHz)	200, 320
FPGA registers/LUTs	20%/22%
FPGA block RAM	40%
FPGA 48-bit multipliers	16%

Table 4. FPGA implementation summary for the correlator.

# 4. ENGINEERING COMMISSIONING RESULTS

The BETA instrument is currently undergoing engineering commissioning trials on site at the Murchison Radio Observatory (MRO) in remote Western Australia. Figure 5 shows the magnitude plot of a typical PAF array covariance matrix for a single 1MHz coarse channel. Note the 94 x 94 X-polarization covariance sub matrix in the upper left and the 94 x 94 Y-polarization covariance submatrix in the lower right. (The color axis is a log scale.)

The image in Figure 6 is the first multi-beam image created using visibilities generated from the BETA DSP system and is proof of the ability of the PAF to observe much larger areas of sky than conventional instruments. The image was created from a 12-hour observation with 9 overlapping beam pairs. The image shows three bright extragalactic sources PKS1610-771, PKS 1549-790 and PKS 1547-795. The contour shows the 50% sensitivity region for the 9-beam configuration.



Figure 5. 188 x 188 Array Covariance Matrix.



Figure 6. Multi-beam image.

### **5. CONCLUSION**

The BETA prototype development has been a critical step in learning how to design the DSP heart of this new class of radio telescope. The many lessons learned in the research and development effort to produce BETA have now fed into the design of the full ASKAP instrument [12] and as BETA continues to provide a valuable engineering test-bed for PAF-based radio astronomy, ASKAP is now beginning to move into the full production phase.

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