EFFICIENT DUTY-CYCLE MISMATCH COMPENSATION IN DIGITAL TRANSMITTER

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ABSTRACT

This paper presents an efficient mitigation approach for duty cycle mismatch of in-phase and quadrature upconversion signals in digital transmitters. This approach is supported by a mathematical analysis of the baseband equivalent impact of duty cycle mismatch. An efficient digital pre-distortion method is proposed to eliminate the distortion impact. Simulation results show that, for both 64-QAM and 256-QAM modulation schemes, the error-vector-magnitude can be improved from -25.1dB to less than -55dB, which leaves substantial design margin for other non-idealities distorting the transmitted signal.

Index Terms— digital mixing, pre-distortion, duty cycle mismatch, digital intensive transmitter

1. INTRODUCTION

The introduction of Software Defined Radio (SDR) requires a wideband transmitter which is capable of combining multiple functionalities and wideband operation while meeting stringent linearity requirements. Besides the demanding requirements imposed by multiple standards, the decreasing supply voltage of modern deep-submicron CMOS technologies challenges the design of the analog circuit even more [1]. To circumvent this, digitized multimode transmitters are being introduced [1]-[6], as shown in Fig.1 (a). These convert the digital baseband signal to its radio frequency (RF) counterpart directly via a single mixed-signal circuit block, called RFDAC, and can take full advantage of increasing speed and decreasing cost of digital signal processing with technology scaling. The versatility and robustness achieved with compact digital signal processing make this direct-digital-to-RF-modulation (DDRM) architecture a preferable solution for a low-cost, multimode transmitter design in deep-submicron CMOS technologies.

Several design challenges arise in the traditional DDRM architectures: 1.) As shown in Fig.1 (b), the RFDAC building block normally adopts the current-steering (CS) architecture and contains an array of parallel unit conversion cells for both in-phase (I) and quadrature (Q) signals. The segmentation level between binary decoding and thermometer decoding sets a distinct tradeoff between the linearity performance and circuit complexity. The transistor matching constraints, determining the linearity performance, can be more relaxed when more bits are encoded in the thermometer scheme, however circuit implementation complexity and power consumption doubles for each added bit; 2.) Timing accuracies of multiphase clocks depend on the matching among active transistors. With decreasing technology size, the mismatch among active devices with dimensions at nano-scale level worsens. The duty cycle mismatch of the square-wave local oscillator (LO) signals in the I and Q branches of the transmitter acts as a severe distortion impact on the error-vector-magnitude (EVM) of output signal.

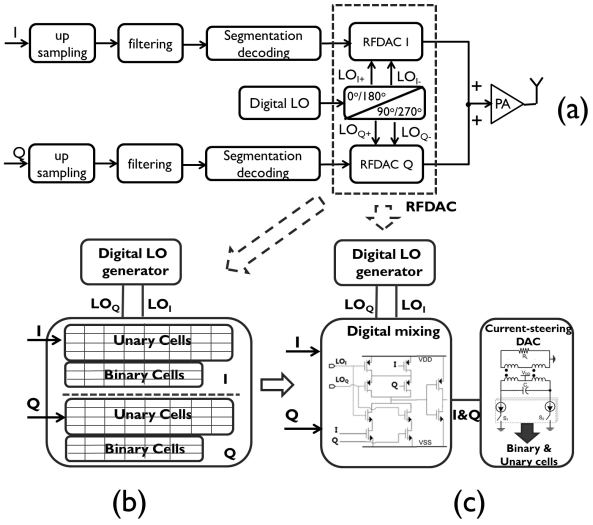

Fig. 1. Architecture of digital transmitter

An alternative RFDAC architecture to tackle the first challenge is shown in Fig.1(c), which features a separate digital quadrature mixing block before digital-to-analog conversion. Since the I and Q signals are coupled together to switch the unit conversion cells in the CS DAC, the number of needed cells is reduced by half. The power consumption can be significantly reduced accordingly, because the unit cells are operating at RF frequency. However, as we will explain in Section 2, in this architecture it is challenging to correct duty cycle mismatch between I and Q LO signals.

This paper first quantitatively analyzes the influence of

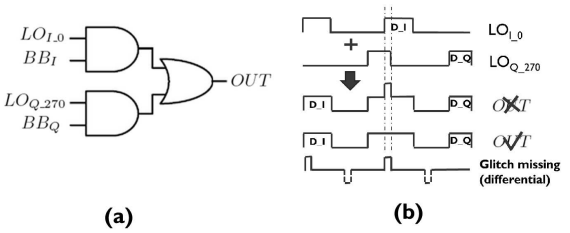

Fig. 2. (a) Functional logic and (b) signal waveforms of mixing cell

duty cycle mismatch in Section 2, especially in the context of digital mixing, and presents the proposed pre-distortion scheme in Section 3; The simulated performance and analysis are reported in Section 4 to prove the effectiveness of the proposed method; Section 5 concludes the paper.

2. ANALYSIS OF DUTY CYCLE MISMATCH

This section analyzes the impact of duty cycle mismatch between I and Q LOs in digital transmitter (DTX) with digital mixing (Fig.1(c)). Two duty cycle mismatch scenarios are studied: 1.) non-overlapping phases; 2.) overlapping phases.

2.1. Non-overlapping phases

The digital mixer combines the LO signal with the digital baseband signal, to steer the current cells in CS RFDAC. One mixing cell exists for each digital input bit with function equivalent to Fig.2(a):

$$OUT = BB_I \times LO_{I\_0} + BB_Q \times LO_{Q\_270} \quad (1)$$

For a square wave LO signal with duty cycle τ, amplitude E and period T, its Fourier expansion is shown as Eqn.(2):

$$\begin{aligned} LO(t) &= \sum_{n=-\infty}^{\infty} F_n \times \exp^{(jnwt)} \\ F_n &= \frac{E\tau}{T} \times \frac{sin\frac{n\pi\tau}{T}}{\frac{n\pi\tau}{T}} \times (1-(-1)^n), w = 2\pi/T \end{aligned} \quad (2)$$

As the LO harmonic components will be greatly suppressed before they are sent out, we only consider the fundamental LO component ($n = 1$) here. Eqn.(2) shows that a mismatch in the duty cycle τ leads to different Fourier expansion coefficients. As a result, a duty cycle mismatch between I and Q LO signals is mathematically equivalent to a gain mismatch between both LO signals. The transmitted complex baseband signal $BB(t) = BB_I(t) + jBB_Q(t)$ is subsequently up-converted by these quadrature LOs affected by such gain mismatch. Resulting baseband equivalent distortion can be expressed as [7]-[9]:

$$BB_d(t) = BB(t) + \beta \times BB^*(t) \quad (3)$$

where τ_I and τ_Q are duty cycles of LO_I and LO_Q.

$$\beta = \frac{sin(\tau_I \times \pi/T) - sin(\tau_Q \times \pi/T)}{sin(\tau_I \times \pi/T) + sin(\tau_Q \times \pi/T)}$$

As can be seen from Eqn.(3), I and Q duty cycle mismatch leads to mutual interference between transmitted I and Q signals.

2.2. Overlapping phases

Consider the special case where I and Q bit signals are both set and LO_I and LO_Q have overlap due to duty cycle mismatch, as shown in Fig.2(b). In the digital mixing scheme, the resulting overlapping output waveforms cannot add up, and the mixing function (Eqn.(1)) will not be valid any longer. More specifically, a non-linear distortion will be added to the model derived above. More particular, in this "phase-overlapping" case, an overlapping glitch is erased from the output power. The transmitted RF signal is then expressed by subtracting the erased power from the up-converted transmitted signal, already distorted by LO gain mismatch:

$$\begin{aligned} RF_d(t) = \frac{2}{\pi} & \underbrace{(sin(\frac{\pi\tau_I}{T})cos(wt)BB_I(t) - sin(\frac{\pi\tau_Q}{T})sin(wt)BB_Q(t)}_{Distorted\ \ by\ \ LO\ \ gain\ \ mismatch} \\ & \underbrace{-f(BB(t))\underbrace{sin(\frac{\pi\tau}{T})}_{x}cos(wt+\underbrace{(\frac{\pi\tau_I}{T}-\frac{\pi\tau}{T})}_{y})\ \ )}_{Subtracting\ \ the\ \ power\ \ of\ \ overlapping\ \ glitch} \end{aligned}$$

where τ_I and τ_Q are the duty cycles of LO_I and LO_Q, τ ($\tau = (\tau_I + \tau_Q)/2 - T/4$) denotes the duty cycle of the missing glitch and $f(BB(t))$ calculates the inner product of the transmitted I and Q baseband signals BB_I and BB_Q:

$$\begin{aligned} f(BB(t)) &= \sum_{n=1}^{NB} BB_I(t)[n] \times BB_Q(t)[n] \times 2^{(n-1)} \\ &+ \sum_{n=NB+1}^{N} BB_S(t)[n] \times 2^{(n-1)} \end{aligned} \quad (4)$$

Here, $BB_S(t) = min(BB_I(t), BB_Q(t))$, N is the bit-width of BB_I and BB_Q, NB is the number of least significant bits (LSBs) with binary decoding. This derivation makes it clear that to also cover cases where LO_I and LO_Q have phase overlap, namely $\tau_I + \tau_Q > T/2$, Eqn.(3) should be modified as follows:

$$\begin{aligned} BB_d(t) &= \underbrace{\sqrt{2}sin(\frac{\pi\tau_I}{T})}_{h}BB_I(t) - \underbrace{\sqrt{2}xcos(y)}_{m}f(BB(t)) \\ &\quad + j(\underbrace{\sqrt{2}sin(\frac{\pi\tau_Q}{T})}_{k}BB_Q(t) - \underbrace{\sqrt{2}xsin(y)}_{n}f(BB(t))) \\ &= h \times BB_I(t) - m \times f(BB(t)) \\ &\quad + j(k \times BB_Q(t) - n \times f(BB(t))) \end{aligned} \quad (5)$$

As can be seen from the above analysis, duty cycle mismatch introduces quadrature modulation errors in the transmitted signal. For the "phase-overlapping" case where the introduced distortion depends on the inner product of BB_I and BB_Q, the well-developed IQ gain and phase mismatch compensation method in [7]-[9] cannot work well any more due to the non-linear inter-modulations.

3. PRE-DISTORTION OF DUTY CYCLE MISMATCH IN DIGITAL MIXING

This section explains the proposed duty cycle mismatch pre-distortion scheme in detail.

A pre-distortion block will map the I and Q baseband input signals BB_I and BB_Q to predistorted BB'_I and BB'_Q. The predistorted signals are constructed so that, after passing through the RFDAC with duty cycle mismatch, they have an output with minimum EVM with the original input $BB_I + j \times BB_Q$. Since the distortion impact of the duty cycle mismatch depends on the inner product of I and Q input signals, it is an irregular non-linear function with rapid fluctuation and hence not reversible, the mapping relation from $BB_{I/Q}$ to $BB'_{I/Q}$ cannot be computed directly and explicitly. The alternative of using a look up table is not practical either, due to the interdependency between I and Q. Assuming I and Q baseband input signals with 10-bit resolution, a look up table with size of 20M (1023x1023x10x2) bits would be needed for one duty cycle mismatch situation. The rapid fluctuation of the non-linear impact of the inner product term moreover prevents the use of look up table interpolation for reducing the size of the look up table.

To overcome the issues discussed above, this paper will present a method to compute the optimum pre-distortion values online. This is achieved by computing an optimum $BB'_{I/Q}$ for any input $BB_{I/Q}$ through an iterative and multi-step search. In every search step, up to three alternative $BB'_{I/Q}$ are generated, and their resulting outputs are computed to identify the candidate with the lowest expected distortion, using distortion formula Eqn.(5). To speed up this search, a descent search is performed in a reduced search range.

Numerical simulations allow quantifying the required search range. Fig.3 shows the optimum BB'_I for any possible input BB_I with 10-bit resolution under an assumed duty cycle mismatch of LO_I and LO_Q being 26% and 28% respectively. It can be seen that the optimum BB'_I for one given input BB_I varies with different input BB_Qs, but the biggest variation of BB'_I from the original input BB_I is limited from -33 to +32. This observation that the optimum $BB'_{I/Q}$ is always in a limited distance from the given input $BB_{I/Q}$ allows to introduce an efficient multi-step search method.

Fig.4 depicts the output EVM corresponding to all the possible $BB'_{I/Q}$s for one given input $BB_{I/Q}$ ({325,325} in the Figure). The optimum $BB'_{I/Q}$ with minimum EVM locates at {332,313}. The output EVM increases with increasing deviation of $BB'_{I/Q}$ from the optimum one.

The shape of the EVM plot indicates that we can reach the optimum solution with a steepest descent searching algorithm. Fig.5 summarizes the complete search flow. For searches with step length of 32, three alternatives BB'_Is ($BB_I, BB_I \pm 32$) are evaluated. Taking into account the searches for BB'_Q ($BB_Q, BB_Q \pm 32$), nine combinations

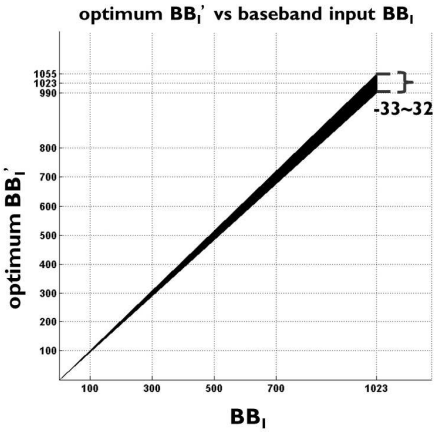

Fig. 3. Optimum BB'_I vs baseband input BB_I

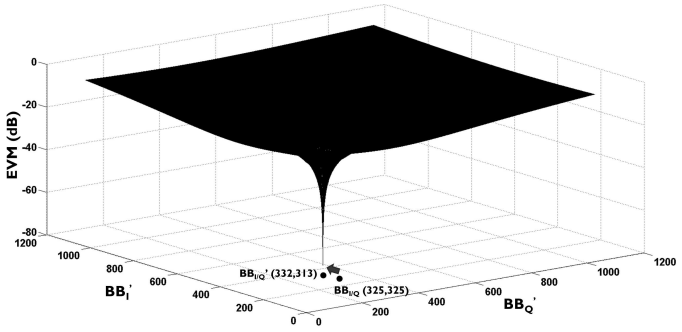

Fig. 4. EVM of the ouput corresponding to all the possible $BB'_{I/Q}$s for one given input $BB_{I/Q}$

will be evaluated to find the $BB'_{I/Q}$ ($BB'_{(I/Q)\_min}$) with minimum EVM in a single such step. Further searches for optimum $BB'_{I/Q}$ will be around $BB'_{(I/Q)\_min}$ with smaller step length from 16 down to 1. E.g., with step length of 16, two $BB'_{I/Q}$s ($BB'_{(I/Q)\_min} \pm 16$) will be evaluated, which corresponds to four search iterations in each step. A trade-off between the number of search iterations and performance is possible by terminating the search before LSB accuracy is reached.

3.1. Estimation of mismatch parameters

As discussed, every evaluation in this search requires the online execution of the distortion formula Eqn.(5), whose mismatch parameters (h, m, k, n) hence have to be estimated first. This can be done by off-line transmission a sequence of training signals and detecting the corresponding output via a loop-back path. h, m can be easily achieved by solving the following matrix equation:

$$\begin{bmatrix} \Re(BB_d(1)) \\ \Re(BB_d(2)) \end{bmatrix} = \begin{bmatrix} BB_I(1) & -f(BB(1)) \\ BB_I(2) & -f(BB(2)) \end{bmatrix} \times \begin{bmatrix} h \\ m \end{bmatrix} \quad (6)$$

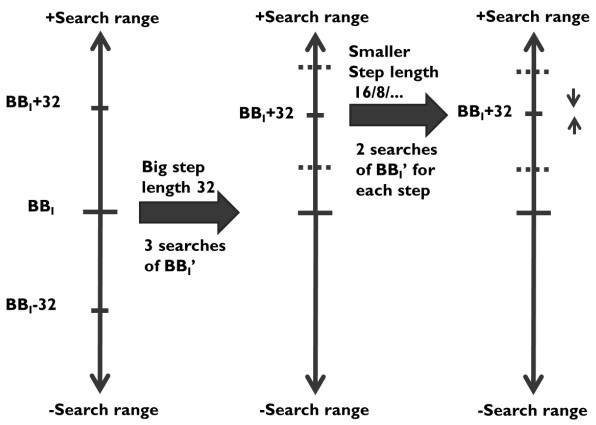

Fig. 5. Proposed search flow

where BB_I is the real part of the transmitted training signal and BB_d is the corresponding baseband equivalent output. The calculation of parameters k, n follows the same rule but operates on the imaginary part.

4. SIMULATION PERFORMANCE AND ANALYSIS

In this section, the performance of various search options is presented in terms of output EVM. Moreover, a validation with real-circuit simulation in the loop is conducted, using Cadence Virtuoso, to show the effectiveness of the proposed pre-distortion scheme under realistic circumstances.

The simulation assumes an OFDM system with 64-QAM modulated symbols. Complex AWG noise which is 60dB lower than the transmitted signal is added to the baseband-equivalent signal to simulate the thermal noise. Large duty cycle mismatch of 26% for LO_I and 28% for LO_Q is injected. As can be seen from Fig.6(c), the output EVM increases 34.3dB due to duty cycle mismatch to -25.2dB. This already violates the specification, since the allowed relative constellation error should not be over -27dB for 64-QAM modulated signal [10]. For the DTX, various significant random and gradient non-idealities still exist in the following CS DAC [11]-[15]. This requires a substantial design margin to the specification before the transmitted signal is further distorted by the non-idealities in CS DAC. As shown in Fig.6(c), after applying pre-distortion with 17 search iterations, over 19dB's $(-27-(-46.1))$ design margin is retained. After 25 search iterations, another 10dB design margin can be gained. Simulation with 256-QAM modulation shows a parallel performance, as shown in Fig.6(d), since the proposed pre-distortion has no dependence on the modulation scheme.

As this paper is the first work to explore the distortion of duty cycle mismatch in digital mixing in DTX, no other alternatives can be found in the literature as comparison. To prove the robustness of the proposed pre-distortion scheme, simulation with a real circuit-level RFDAC is conducted. A single tone input at 2 MHz with 64-QAM modulation and

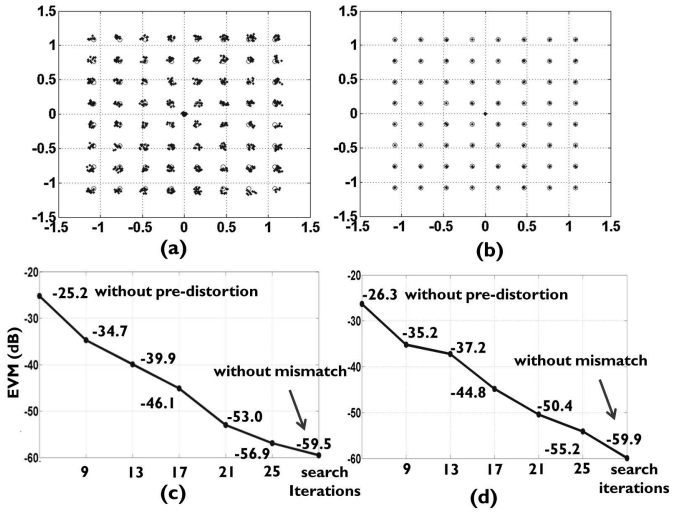

Fig. 6. 64-QAM constellation distorted by duty cycle mismatch (a) and after pre-distortion with 25 search iterations (b); EVM performance for 64-QAM (c) and 256-QAM (d).

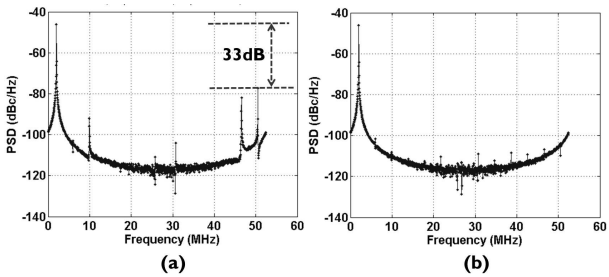

Fig. 7. PSD results before (a) and after (b) mismatch pre-distortion in the real-circuit simulation.

10-bit quantization are assumed in the digital baseband signal generation. The whole RFDAC block, including the segmentation decoding, digital mixing with duty cycle mismatch and CSDAC, are simulated at circuit level in Cadence Virtuoso. Spectrum analysis of the output in Fig.7(a) shows that, without pre-distortion, significant unwanted images are generated due to the duty cycle mismatch. Applying the pre-distortion with 21 search iterations, all the images can be reduced to the noise floor.

5. CONCLUSIONS

This paper analyzes the impact of the duty cycle mismatch in digital transmitters with digital mixing. An effective digital pre-distortion scheme is proposed to eliminate the distortion on the output, capable of pushing the output EVM below -55dB for both 64-QAM and 256-QAM modulation. This is needed to leave substantial design margin for the transmitted signal further distorted by other non-idealities.

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