A 3.8 Gb/s LARGE-SCALE MIMO DETECTOR FOR 3GPP LTE-ADVANCED

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ABSTRACT

This paper proposes—to the best of our knowledge—the first ASIC design for high-throughput data detection in single carrier frequency division multiple access (SC-FDMA)-based large-scale MIMO systems, such as systems building on future 3GPP LTE-Advanced standards. In order to substantially reduce the complexity of linear soft-output data detection in systems having hundreds of antennas at the base station (BS), the proposed detector builds upon a truncated Neumann series expansion to compute the necessary matrix inverse at low complexity. To achieve high throughput in the 3GPP LTE-A uplink, we develop a systolic VLSI architecture including all necessary processing blocks. We present a corresponding ASIC design that achieves 3.8 Gb/s for a 128 antenna, 8 user 3GPP LTE-A based large-scale MIMO system, while occupying 11.1 mm^2 in a TSMC 45 nm CMOS technology.

Index Terms— Large-scale (or massive) MIMO, linear soft-output detection, Neumann series, ASIC design.

1. INTRODUCTION

1.1. Large-scale MIMO

Large-scale (or massive) MIMO postulates the use of antenna arrays having hundreds of antennas at the base station (BS), while serving tens of users simultaneously and in the same frequency band [2]. This technology promises significant improvements in terms of spectral efficiency, link reliability, and coverage over conventional (small-scale) MIMO systems [2–5]. The benefits of large-scale MIMO, however, come at the cost of significantly increased computational complexity at the BS compared to small-scale MIMO systems (e.g., systems equipped with six or fewer antennas). In addition, cellular systems, such as 3GPP LTE [6] or LTE Advanced (LTE-A) [7], rely on single carrier frequency division multiple access (SC-FDMA) which further increases the dimensionality of the underlying detection problem. Hence, optimal detection methods, such as maximum-likelihood (ML) detection [8] or soft-output sphere decoding (SD) [9, 10], whose computational complexity scales exponentially in the number of transmit streams [11, 12] result in prohibitive complexity. Consequently, low-complexity (but sub-optimal) detection schemes [3] that scale favorably to the high-dimensional detection problems faced in SC-FDMA-based large-scale MIMO systems are necessary in practice.

An extended version of this paper detailing an FPGA design will appear in [1]. This work was supported in part by the US National Science Foundation under grants CNS-1265332, ECCS-1232274, and CNS-0923479.

1.2. Contributions

We propose—to the best of our knowledge—the first application specific integrated circuit (ASIC) for the uplink in SC-FDMA-based large-scale MIMO systems, i.e., where multiple users communicate with the BS. To significantly reduce the computational complexity of linear soft-output detection, we build our detector upon the truncated Neumann series expansion method for approximate maxxtrix inversion developed in [13, 14]. We present a corresponding systolic VLSI architecture that is able to achieve high throughput at low silicon area, even for very large BS antenna arrays. The resulting ASIC design for a TSMC 45 nm CMOS technology achieves a peak uplink throughput of 3.8 Gb/s in a 128 antenna, 8 user scenario, exceeding the 1.5 Gb/s peak uplink rate specified in LTE-A operating at 100 MHz bandwidth [7].

2. APPROXIMATE SOFT-OUTPUT DETECTION IN THE LARGE-SCALE MIMO LTE-A UPLINK

2.1. SC-FDMA uplink model

We consider an SC-FDMA-based large-scale multi-user MIMO uplink with B antennas at the BS communicating with $U \leq B$ single-antenna users. The i^{th} user first maps the coded bit stream onto constellation points in a finite alphabet $\mathcal{O}$ (such as QPSK or 16-QAM) with average power of E_s per symbol. A discrete Fourier transform (DFT) block then transforms each L group of constellation points, $\mathbf{x}^{(i)} = \left[x_1^{(i)}, \ldots, x_L^{(i)}\right]^T$, into DFT modulated symbols $\mathbf{s}^{(i)} = \left[s_1^{(i)}, \ldots, s_L^{(i)}\right]^T$. These symbols are mapped onto L data-carrying subcarriers and transmitted by the user. At the BS, the received symbols in the frequency domain on the w^{th} subcarrier are modeled as $\mathbf{y}_w = \mathbf{H}_w \mathbf{s}_w + \mathbf{n}_w$. Here, the vector $\mathbf{y}_w = \left[y_w^{(1)}, \ldots, y_w^{(B)}\right]^T$ contains symbols received at the base-station antennas on the w^{th} subcarrier.

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The vector $\mathbf{s} = \left[s_w^{(1)}, \ldots, s_w^{(U)}\right]^T$ contains the symbols transmitted by the users simultaneously on the w^{th} subcarrier. The $B \times U$ matrix $\mathbf{H}_w$ contains the channel gains between the receive antennas and transmit antennas on the w^{th} subcarrier, and $\mathbf{n}_w = \left[n_w^{(1)}, \ldots, n_w^{(B)}\right]^T$ models thermal noise at the w^{th} subcarrier in the frequency domain. The entries of the vector $\mathbf{n}_w$ are assumed to be i.i.d. zero-mean complex Gaussian random variables with variance N_0 per complex entry.

2.2. Linear soft-output MMSE detection

To arrive at low computational complexity for data detection in SC-FDMA-based large-scale MIMO systems, we focus on linear soft-output detection. Linear soft-output detection for SC-FDMA mainly consists of the following two steps: (i) *channel equalization* to generate estimates of the frequency domain symbols, and (ii) *soft-output computation* to generate LLRs from the equalized frequency domain symbols.

For channel equalization, we apply a minimum-mean square error (MMSE) equalizer on a per-subcarrier basis in the frequency domain. To reduce the amount of recurrent computations [15], we first compute the matched-filter (MF) outputs as $\mathbf{y}_w^{\text{MF}} = \mathbf{H}_w^H \mathbf{y}_w$ and the Gram matrices $\mathbf{G}_w = \mathbf{H}_w^H \mathbf{H}_w$ for each subcarrier, followed by forming the regularized Gram matrix $\mathbf{A}_w = \mathbf{G}_w + N_0 E_{\text{s}}^{-1} \mathbf{I}_U$. The equalized symbols per subcarrier are computed as $\hat{\mathbf{s}}_w = \mathbf{A}_w^{-1} \mathbf{y}_w^{\text{MF}}$, which requires an $U \times U$-dimensional matrix inversion; this inversion causes most of the detector's complexity.

For soft-output computation, we model the estimated t^{th} symbol transmitted from the i^{th} user as $\hat{x}_t^{(i)} = \mu^{(i)} x_t^{(i)} + e_t^{(i)}$, where $\mu^{(i)}$ is the effective channel gain and $e_t^{(i)}$ is the post-equalization noise-plus-interference with variance ν_i^2. By defining $\rho_i^2 = \left(\mu^{(i)}\right)^2 / \nu_i^2$ as the post-equalization signal-to-noise-plus-interference ratio (SINR) and b as the bit index of the LLR associated with the t^{th} symbol transmitted from the i^{th} user, we can compute the max-log LLRs as [15]

$$L_t^{(i)}(b) = \rho_i^2 \left(\min_{a \in \mathcal{O}_b^0} \left| \frac{\hat{x}_t^{(i)}}{\mu^{(i)}} - a \right|^2 - \min_{a' \in \mathcal{O}_b^1} \left| \frac{\hat{x}_t^{(i)}}{\mu^{(i)}} - a' \right|^2 \right), \quad (1)$$

where $\mathcal{O}_b^0$ and $\mathcal{O}_b^1$ correspond to the sets of constellation symbols for which the b^{th} bit equals to 0 and 1, respectively.

2.3. Approximate MMSE detection via Neumann series

For SC-FDMA-based large-scale MIMO systems with a large number of users U, computation of the inverse $\mathbf{A}_w^{-1}$ can result in significant computational complexity. Hence, to reduce the complexity of computing the inverse $\mathbf{A}_w^{-1}$, we use the following Neumann series expansion [16]:

$$\mathbf{A}_w^{-1} = \sum_{n=0}^{\infty} \left(\mathbf{X}^{-1} \left(\mathbf{X} - \mathbf{A}_w \right) \right)^n \mathbf{X}^{-1}. \quad (2)$$

By decomposing $\mathbf{A}_w$ such that $\mathbf{A}_w = \mathbf{D}_w + \mathbf{E}_w$, where $\mathbf{D}_w$ is the main diagonal of $\mathbf{A}$ and $\mathbf{E}_w$ is the hollow regularized Gram matrix, we can approximate the inverse $\mathbf{A}_w^{-1}$ by keeping only the first K terms of the Neumann series [13, 14]

$$\widetilde{\mathbf{A}}_{w\,|\,K}^{-1} = \sum_{n=0}^{K-1} (-\mathbf{D}_w^{-1} \mathbf{E}_w)^n \mathbf{D}_w^{-1}, \quad (3)$$

which can be computed at (often significantly) lower computational complexity than an exact inverse for $K \leq 3$.

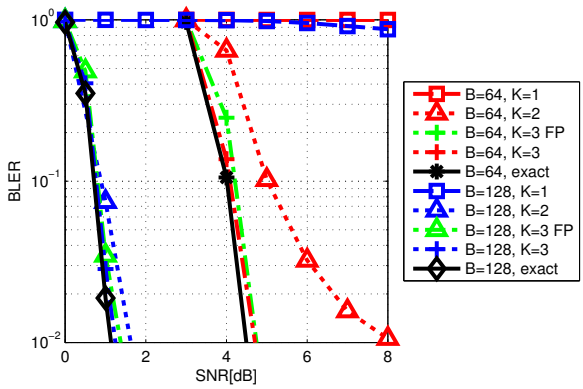

Fig. 1. Block error-rate (BLER) performance for $U = 4$ single-antenna users; 'FP' indicates fixed-point performance.

Computation of the max-log LLRs (1) using (3) is carried out by replacing the exact inverse $\mathbf{A}_w^{-1}$ by the approximation $\tilde{\mathbf{A}}_{w\,|\,K}^{-1}$. With this approximation, the effective channel gain $\tilde{\mu}_K^{(i)}$ and the variance of the residual post-equalization NPI variance $\tilde{\nu}_{i\,|\,K}^2$ now depend on the number of Neumann series terms. To reduce complexity, we propose to use the effective channel gain and residual post-equalization NPI variance of the 1-term approximation. With this approximation, the effective frequency domain channel gain at the w^{th} subcarrier for the K term approximation is given by $\widetilde{\mathbf{H}}_{w|1} = \mathbf{D}_w^{-1} \mathbf{H}_w^H \mathbf{H}_w$. Further, by exploiting properties of the IDFT, the time domain channel gain of the i^{th} user is $\tilde{\mu}_K^{(i)} = L^{-1} \sum_{w=1}^{L} \tilde{h}_{w|1}^{(i,i)}$, where $\tilde{h}_{w|K}^{(i,i)}$ is the i^{th} diagonal entry of $\widetilde{\mathbf{H}}_{w|1}$. We also approximate the noise-plus-interference variance as follows:

$$\tilde{\nu}_i^2 \approx E_s \sum_{w=1}^{L} (d_w^{(i,i)})^{-1} g_w^{(i,i)} - E_s |\tilde{\mu}_1^{(i)}|^2. \quad (4)$$

Here, $d_w^{(i,i)}$ is the i^{th} diagonal entry of $\mathbf{D}_w$, and $g_w^{(i,i)}$ is the i^{th} diagonal entry of $\mathbf{G}_w$. Note that the NPI approximation (4) performs almost equally well as using the exact NPI variance.

2.4. Simulation results

To characterize the performance of the proposed algorithms, we consider modulation and coding scheme (MCS) 28 with a bandwidth of 20 MHz and 1200 data carrying subcarriers, as specified by the LTE standard [6]; this mode corresponds to 64-QAM, and a rate 0.75 turbo code. The channel matrices are generated using the WINNER-Phase-2 model [17], where we use a linear antenna array with spacing of $10\,\text{m}/128 \approx 0.781\,\text{m}$, similar to the channel measurement

campaign in [18]. At the BS, we perform exact as well as approximate soft-output MMSE detection. We furthermore use a log-MAP LTE turbo decoder performing 16 (full-)iterations. Figure 1 shows the block-error rate (BLER) performance of the proposed approximate detection algorithm compared to that of an exact MMSE detector for $U = 4$. The proposed method with $K = 3$ approaches the performance of the exact detector, but at significantly lower computational complexity.

3. VLSI ARCHITECTURE

3.1. Architecture overview

The proposed VLSI architecture is illustrated in Fig. 2. The detector consists of three main units: (i) the preprocessing unit, (ii) the subcarrier processing unit, and (iii) the user processing unit. The preprocessing unit performs matched filtering $\mathbf{y}_w^{\text{MF}} = \mathbf{H}_w^H \mathbf{y}_w$ and computes the regularized Gram matrix $\mathbf{A}_w$ as well as the corresponding (approximate) matrix inversion in (3). These results, along with intermediate values $\mathbf{D}_w^{-1}$ and $\mathbf{G}_w$, are then passed to the subcarrier processing unit. This unit performs equalization, i.e., computes $\hat{\mathbf{s}}_w = \widetilde{\mathbf{A}}_{w\,|\,K}^{-1} \mathbf{y}_w^{\text{MF}}$ and the post-equalization SINR at each subcarrier. Since data detection is carried out for each user, a data buffer is required to convert all equalized symbols and SINR values from a per-subcarrier basis to a per-user basis. The user processing unit converts the equalized symbols for each user into the time domain using an IFFT block and generates soft-output information in the form of max-log LLRs using the buffered post-equalization NPI values. We note that the preprocessing unit operates at symbol rate as channel estimates may change from symbol to symbol in LTE systems [19]. To meet the LTE-A peak throughput, we use multiple instances of the preprocessing unit. We next provide the details for the two most crucial blocks. The architectures of the remaining blocks are straightforward.

3.2. Approximate matrix inversion unit

Figure 2 shows the triangular systolic array used for computing the Gram matrix and the K-term Neumann series approximation. The systolic array consists of two processing elements (PEs): PEs on the diagonal of the systolic array (PE-D) and PEs on the off-diagonal (PE-OD). Both PEs have different modes in the four computation phases summarized next.

First phase: This phase first computes the $U \times U$ regularized Gram matrix $\mathbf{A}_w = \mathbf{G}_w + N_0 E_s^{-1} \mathbf{I}_U$ as well as $\mathbf{D}_w^{-1}$ using reciprocal units (denoted by *inv* in Fig. 2) in the PE-D units. Since $\mathbf{A}_w$ is diagonally dominant with diagonal values close to B, we mitigate dynamic-range issues by the *scale down* unit. The results $\mathbf{D}_w^{-1}$ and $\mathbf{E}_w$ are stored in distributed register files for the subsequent phases.

Second phase: The systolic array computes $-\mathbf{D}_w^{-1}\mathbf{E}_w$ using $\mathbf{D}_w^{-1}$ and $\mathbf{E}_w$ obtained in the first phase. Since the matrix $-\mathbf{D}_w^{-1}\mathbf{E}_w$ is not Hermitian, the systolic array computes the upper- and lower-triangular part of $-\mathbf{D}_w^{-1}\mathbf{E}_w$ separately. As $\mathbf{D}_w^{-1}$ is diagonal, computation of $-\mathbf{D}_w^{-1}\mathbf{E}_w$ only requires a series of scalar multiplications.

Third phase: The systolic array computes the 2-term Neumann series approximation: $\widetilde{\mathbf{A}}_{w\,|\,2}^{-1} = \mathbf{D}_w^{-1} - \mathbf{D}_w^{-1}\mathbf{E}_w\mathbf{D}_w^{-1}$. Since $\mathbf{D}_w^{-1} - \mathbf{D}_w^{-1}\mathbf{E}_w\mathbf{D}_w^{-1}$ is Hermitian, only the lower-triangular part needs to be computed. Furthermore, since $\mathbf{D}_w^{-1}$ is diagonal, computation of $-\mathbf{D}_w^{-1}\mathbf{E}_w\mathbf{D}_w^{-1}$ only requires entry-wise multiplications. The computation is carried out by loading $\mathbf{D}_w^{-1}$ and $-\mathbf{E}_w\mathbf{D}_w^{-1}$ into all PEs and performing scalar multiplications. We then add $\mathbf{D}_w^{-1}$ to the result in the diagonal PE and store the result $\mathbf{D}_w^{-1} - \mathbf{D}_w^{-1}\mathbf{E}_w\mathbf{D}_w^{-1}$ in the distributed register files.

Fourth phase: In this phase, the systolic array iteratively computes a K-term Neumann series approximation using the $(K-1)$-term approximation residing in the distributed register files. The systolic array performs a matrix multiplication of $-\mathbf{D}_w^{-1}\mathbf{E}_w$ with $\widetilde{\mathbf{A}}_{w\,|\,K-1}^{-1}$ and then, adds $\mathbf{D}_w^{-1}$ to the diagonal PE. The resulting K-term approximation $\widetilde{\mathbf{A}}_{w\,|\,K}^{-1}$ is then stored in the register files. Since we can repeat this phase for a configurable number of iterations, we can compute an arbitrary K-term approximation with the same systolic array.

3.3. IFFT and LLR computation unit

In order to transform the per-subcarrier data into the user (or time) domain, we use an IFFT to support 3GPP LTE [6] standard. The core supports the transform size of $L = 2^x 3^y 5^z$, which consists of Radix-2, Radix-3, and Radix-5 operations. The IFFT unit reads and outputs complex data in serial manner, and achieves a throughput well-beyond 1.9 Gb/s for 8 users, 64-QAM, and 100 MHz bandwidth.

The LLR computation unit computes (1) given the effective channel gains $\mu^{(i)}$ from the IFFT block and the post-equalization SINR values ρ_i^2 obtained from the SINR block. Since LTE specifies Gray mappings for all modulation schemes, LLR computation is accomplished at low complexity (see [15] for the details). A single instance of this unit is able to processes one symbol every clock cycle, resulting in a throughput of 6 Gb/s for 64-QAM when running at 1 GHz.

4. ASIC IMPLEMENTATION

4.1. Fixed-point design parameters

The proposed design is implemented with fixed-point arithmetic to minimize the hardware complexity and to maximize the throughput. The channel matrices $\mathbf{H}_w$, receive vectors $\mathbf{y}_w$, matched filter outputs $\mathbf{y}_w^{\text{MF}}$, approximate inverses $\widetilde{\mathbf{A}}_{w\,|\,K}^{-1}$, and the Gram matrices $\mathbf{G}_w$, are represented by 15 bit for real and imaginary parts, respectively. All multiplier units use 22 bit precision, except in the FFT unit, which uses 18 bit precision. To reduce the size of the data buffer, we quantize its contents to 12 bit. The inputs and outputs of the IFFT and of the LLR computation unit use 12 bit. The negligible BLER

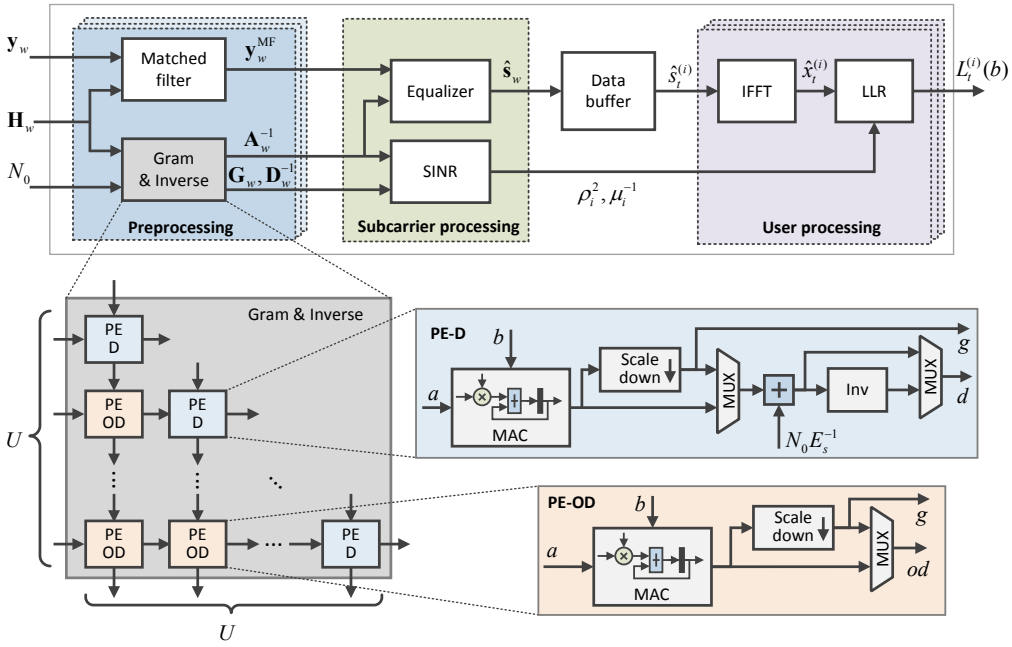

Fig. 2. High-level VLSI architecture of the approximate MIMO detector for large-scale 3GPP LTE-A systems.

Antenna configuration	128 BS antennas, 8 users
Inversion algorithm	$K = 3$ term approximation
Technology	TSMC 45nm CMOS
Max. clock frequency	1 GHz
Throughput	3.8 Gb/s
Core area (utilization)	11.1 mm^2 (73 %)
Cell area (excluding memories)	12.6 MGE
Memory size (ROM & RAM)	1 050 Kb
Power consumption	8 W @ 1 GHz and 0.81 V

Table 1. Post-layout implementation results of the proposed approximate MIMO detector for large-scale 3GPP LTE-A.

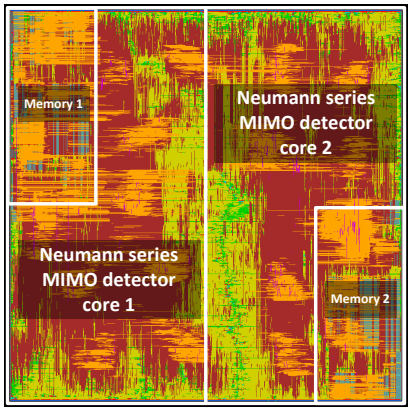

Fig. 3. ASIC layout of the dual-core large-scale MIMO detector for 3GPP LTE-A in TSMC 45nm CMOS technology

performance loss resulting from fixed-point precision artifacts is shown in Fig. 1.

4.2. Implementation results

Table 1 summarizes the key (post-layout) characteristics of the implemented approximate MIMO detector for large-scale 3GPP LTE-A in TSMC 45nm CMOS technology. In order to meet the uplink throughput specified in 3GPP LTE-A for a 8 user, 128 BS antenna system, we need two instances of the detector. Each detector consists of 8 preprocessing units, 1 subcarrier processing unit, and 1 user processing unit. The layout of the resulting dual-core ASIC is shown in Fig. 3 and occupies a total of 12.6 MGE and 11.1 mm^2. Note that all RAMs and ROMs (for the data buffer, the IFFT's twiddle factors, and the reciprocal units) have been generated using the ARM memory compiler [20]. The final design achieves a peak throughput of 3.8 Gb/s, which exceeds the 1.5 Gb/s peak data rate of LTE-A with 4 users and 100 MHz bandwidth, as it supports data detection for up to 8 users communicating concurrently and in the same frequency band.

To the best of our knowledge, there are no existing large-scale MIMO detector designs for LTE-A. Existing LTE uplink detectors [21–25] are designed for small-scale MIMO systems and are, hence, significantly less complex, which prohibits a fair comparison to our ASIC design. We emphasize that our design demonstrates the feasibility of using large-scale MIMO in future 3GPP LTE-A standards, even when having hundreds of antennas at the BS. The development of improved (e.g., non-linear) detection methods and corresponding VLSI/ASIC designs is part of on-going work.

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