PARTIAL CRC-ASSISTED ERROR CORRECTION OF AIS SIGNALS RECEIVED BY SATELLITE

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ABSTRACT

This paper deals with the demodulation of automatic identification system (AIS) signals received by a satellite. More precisely, an error correction algorithm is presented, whose computational complexity is reduced with respect to that of a previously considered approach. This latter approach makes use of the cyclic redundancy check (CRC) of a message as redundancy, in order to correct transmission errors. In this paper, the CRC is also considered as a correction tool, but only a part of it is used for that purpose; the remaining part is only used as an error detection means. This novel approach allows the decoding performance to be adapted to the noise power, and provides a reduction of the computational complexity. Simulation results obtained with and without complexity optimization are presented and compared in the context of the AIS system.

***Index Terms*—** AIS, satellite, CRC, Viterbi decoding, optimization.

1. INTRODUCTION

The objective of this paper is to present an optimized demodulation algorithm of automatic identification system (AIS) signals received by satellite. The AIS is a radio communication system primarily designed as a collision avoidance system for large vessels. This system consists of periodically emitting short bursts broadcasted in VHF [1]. Although this system was not primarily conceived for satellite reception, it is possible to demodulate AIS signals recorded by a satellite for maritime traffic surveillance. Some systems are already operational [2], and studies devoted to improve the detection performance are still in progress [3–8]. In a previous work [9], we proposed to use the cyclic redundancy check (CRC) as an error correction tool in order to optimize the demodulation rate at low E_S/N_0. The algorithm studied in [9] assumed a perfect phase recovery and no message collision. Further investigations have been proposed to consider interference mitigation [10] and phase shift estimation and tracking [11]. However, the resulting algorithm had a significant computational complexity. Even if a real-time processing is not required, reducing this complexity is interesting, which is the objective of this paper. The complexity is essentially due to the large number of states in the Viterbi trellis used to correct transmission errors by exploiting the CRC. This number of states is equal to $4 \cdot 2^{N_{\text{CRC}}}$, where N_{CRC} is the number of CRC bits. The algorithm proposed in this paper reduces the number of CRC bits considered for error correction and thus the number of states of the Viterbi trellis. By using this new algorithm, instead of using the whole 16-bit CRC of the AIS system, it becomes possible for instance to use only 8 CRC bits for error correction, while the remaining 8 bits are used for error detection only. Hence, the number of states is reduced by a factor of $2^8 = 256$, leading to a considerable speed up of the algorithm. In this paper, we propose an adaptive complexity scheme which iteratively increases the portion of the CRC used for error correction, until no error is detected.

The approach proposed in [9] is based on a Viterbi algorithm relying on a particular trellis. This trellis, referred to as extended trellis, is composed of the trellis of the intermediate CRC values and the coding trellis. Moreover, the stuffing bit procedure affecting AIS signals is taken into account by including specific transitions in the extended trellis. More details about this algorithm can be found in [9, 12, 13]. The main contribution of this work is to elaborate a reduced trellis by considering only a part of the CRC to construct the extended states. The actual value of the CRC computed along the path through the trellis is registered in a state variable and is used to compute the next CRC state during a transition. The phase tracking procedure proposed in [11] and the correction enhancement strategy proposed in [14] remain applicable to the proposed receiver. Note that the proposed partial CRC-based error correction strategy could also be applied to other systems involving CRC and bit stuffing, such as the universal serial bus (USB), high level data link control (HDLC) or X.25 systems [9].

The paper is organized as follows. The transmitter characteristics and the received signal model are presented in section 2. Section 3 describes the demodulation algorithm with a specific attention to the proposed complexity optimization, which constitutes the main novelty of this paper. Some simulation results are given in section 4 illustrating the performance of the proposed approach using a realistic AIS simulator, developed by the CNES (French national space agency) of Toulouse, France. Conclusions are reported in Section 5.

2. TRANSMITTER DESIGN

This paper considers only single-user AIS transmissions. Although the interference mitigation strategy described in [10] could be applied, it will not be presented in this paper for brevity. AIS messages are composed of 168 information bits, from which a 16-bit CRC is computed. The CRC is concatenated to the information bits and the bit stuffing procedure is applied on the resulting sequence. The sequence obtained after bit stuffing is then transmitted by using NRZI

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coding and GMSK modulation. Some properties of each step of the transmitter design are recalled below.

2.1. Cyclic redundancy check properties

The CRC is defined as the division (modulo 2) of the polynomial derived from the data and a standardized generator polynomial. To obtain a fixed-length CRC, zeros are inserted before the remainder. It is well known that the CRC can also be computed iteratively by initializing the CRC to a standard value and by applying operations sequentially to each data bit. The diagram of the iterative operator is presented in [9]. This iterative property allows a CRC computing trellis to be developed, whose states represent the intermediate values of the CRC computation. CRCs are generally used to detect transmission errors by comparing the CRC computed from the received data and the CRC contained in the data frame. An equivalent way to detect transmission error is to consieder the overall joint CRC computed from the data concatenated to the CRC. Indeed, no transmission error is detected when this joint CRC is zero, i.e.,

$$\text{CRC}([\text{Data}, \text{CRC}(\text{Data})]) = 0. \tag{1}$$

As shown in [9, 12, 13], the CRC can be used as an error correction means. Indeed, the CRC is the result of a calculation on the data, and then contains a part of the information. In this paper, one part of the CRC is used to correct transmission errors, while the other part is used as an error detection tool.

2.2. Bit stuffing procedure

The bit stuffing procedure in AIS system consists of the insertion of a non informative bit 0 after any sequence of five consecutive bits 1. This procedure avoids the presence of long sequences of bits 1 that could cause a loss of clock synchronization. Also, the inserted bits 0 prevent the presence of end frame flags inside the data. These flags are composed of two bits 0 on each side of six consecutive bits 1. Hence, the bit stuffing procedure removes the sequences of six bits 1 in the data. Since the stuffing bits are non informative and randomly localized, the receiver must detect and localize them before decoding.

This procedure is the major reason of the proposed corrector complexity. Indeed, because of the presence of stuffing bits, classical low-complexity error correction algorithms are not applicable [9].

2.3. GMSK modulation

After the bit stuffing procedure, the frame is encoded using the non-return-to-zero inverted (NRZI) coding, and modulated with the Gaussian minimum shift-keying (GMSK) modulation. In GMSK, the transmitted signal $s(t)$ is a constant-modulus signal defined as

$$s(t) = e^{-j\theta(t;\mathbf{B})}$$

where the phase $\theta(t;\mathbf{B})$ contains the information symbols

$$\theta(t;\mathbf{B}) = 2\pi h \sum_{k=-\infty}^{n} b_k q(t-kT),\ nT \leqslant t \leqslant (n+1)T. \tag{2}$$

In (2), T is the symbol period, $\mathbf{B} = \{b_k\}$ is the bit sequence, h is the modulation index, and $q(t)$ is the GMSK waveform [1]. In the AIS system, the modulation index is theoretically equal to $h = 0.5$. However, the actual modulation index can be significantly different ($\pm 15\%$ variations can be observed). The estimation of the actual value of h is discussed in [11].

2.4. Received signal model

The transmission channel considered in this paper is a frequency-flat channel with transmission delay and Doppler shift assumed to be known by the receiver. Note that these parameters could be estimated using a correlation with the pilot symbols. Note also that the phase shift can be taken into account by performing the phase tracking procedure of [11]. However phase tracking and parameter estimation are not considered here. Denoting the signal generated by the GMSK modulator by $s(t)$, the received signal can be expressed as

$$r(t) = s(t) + n(t) \tag{3}$$

where $n(t)$ is a white additive Gaussian noise independent of the transmitted signals. The objective of AIS signal demodulation is to recover the information data contained in the signal $s(t)$ from the received signal $r(t)$.

3. RECEIVER DESCRIPTION

3.1. General principle

The receiver considered in this paper uses a modified version of the Viterbi algorithm. This algorithm determines the maximum likelihood symbol sequence from the received signal (3). First, the received signal (3) is passed through a matched filter (MF) and sampled with one sample per symbol denoted r_k for the kth symbol period. Then, the sample sequence is processed by the Viterbi algorithm in which the distance function is the square Euclidean distance

$$\sum_{k=1}^{K} |r_k - m_k|^2 \tag{4}$$

where m_k is the sample of the kth estimated symbol after MF. Because of the possible presence of stuffing bits, the Viterbi algorithm has to be modified in order to consider conditional transitions to satisfy the following constraint: the number of consecutive bits 1 is upper bounded by a value $\overline{P}$, specified by the application standard ($\overline{P} = 5$ for the AIS).

Since the CRC is used as an error corrector tool, a specific constraint has to be defined on the trellis. In [9] the joint CRC was used and constrained to satisfy (1). In this paper only a part of the CRC is used. Thus, only part of the joint CRC is constrained to be zero. Denote as $\widetilde{\text{CRC}}$ the part of the CRC used for error correction. To take into account the constraint $\widetilde{\text{CRC}} = 0$, a so-called extended trellis is developed, whose states (referred to as extended states) are composed of a $\widetilde{\text{CRC}}$ state and a trellis code (TC) state. The final extended state is chosen in order to ensure that $\widetilde{\text{CRC}}$ equals zero to perform the error correction.

Note that the part of the CRC which is not contained in $\widetilde{\text{CRC}}$ could be used for error detection, by comparison to zero in order to check if errors are present in the decoded message.

3.2. Extended trellis construction

Since the CRC (and hence $\widetilde{\text{CRC}}$) can be computed iteratively, it can be initialized to a particular value given by the CRC standard, and then updated at each received bit. In the algorithm proposed in [9], a CRC trellis is developed with CRC states defined as particular intermediate CRC values. Two consecutive CRC states are connected if the second CRC state can be obtained from the first CRC state by including a bit 0 or a bit 1. In this paper, a $\widetilde{\text{CRC}}$ trellis is developed with states representing the first part of the CRC values.

For instance, if each letter a, b, c,... represents any block of 4 bits (note that the whole CRC contains 16 bits in AIS), the $\widetilde{\text{CRC}}$ state denoted **aa** represents all the CRC values beginning with **aa**, i.e., [**aa**aa], [**aa**bb], [**aa**cc]... In the $\widetilde{\text{CRC}}$ trellis, a limited number of bits of the CRC is used to connect two $\widetilde{\text{CRC}}$ states. If the CRC value [**aa**bb] is followed by [**cc**dd] when updated with a bit 0 and by [**ee**ff] when updated with a bit 1, then transitions exist going from the $\widetilde{\text{CRC}}$ state **aa** to $\widetilde{\text{CRC}}$ states **cc** and **ee** as illustrated in Fig. 1.

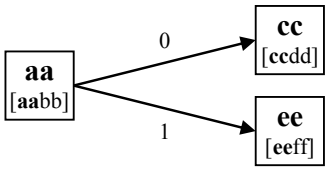

Fig. 1. Construction of the new $\widetilde{\text{CRC}}$ trellis.

Since the full value of the CRC is required to compute the updated CRC value, a new state variable C is defined to register this full CRC value. At each instant of the Viterbi algorithm, the state variable C of a given $\widetilde{\text{CRC}}$ state is used to compute the next possible $\widetilde{\text{CRC}}$ states. The updated full CRC values are registered in the state variable C of these next $\widetilde{\text{CRC}}$ states.

To define an extended state, a $\widetilde{\text{CRC}}$ state is associated with a state of the trellis code (a TC state) and both trellis behave in parallel with the same bits. This mechanism is illustrated in (5), where the integer k corresponds to the kth received symbol.

$$\begin{array}{cccc} \widetilde{\text{CRC}}\text{ state}_{k\ \ k+1} & & \text{TC state}_{k\ \ k+1} & \Rightarrow \quad \text{Extended state}_{k\ \ k+1} \\ A \xrightarrow{0} B & \& & \alpha \xrightarrow{0} \beta & \Rightarrow \quad (A;\alpha) \xrightarrow{0} (B;\beta) \\ A \xrightarrow{1} C & & \alpha \xrightarrow{1} \gamma & \Rightarrow \quad (A;\alpha) \xrightarrow{1} (C;\gamma) \end{array} \tag{5}$$

The number of states associated with the extended trellis equals the product between the number of states of the TC trellis (i.e., 4 for the AIS system) and the number of states of the $\widetilde{\text{CRC}}$ trellis (i.e., $2^{N_{\widetilde{\text{CRC}}}}$ with $N_{\widetilde{\text{CRC}}}$ the number of bits used for error correction).

3.3. Bit stuffing

The stuffing bits are considered in the extended trellis by including specific transitions which can only be used when a stuffing bit is received. The detection of these stuffing bits is done by comparing the state variable P introduced in [9] with 5. The state variable P represents the number of bits 1 received just before reaching the state and 5 is the number of bits 1 leading to the inclusion of a stuffing bit.

Since the stuffing bits are included after the CRC computation on the transmitter side, when one of them is received, the $\widetilde{\text{CRC}}$ state does not change. However, the TC state behaves as if a bit 0 is received.

$$\begin{array}{ll} \text{Information bit} & \text{Stuffed bit} \\ (A;\alpha)_{P=3} \xrightarrow{0}_{k\ \ k+1} (B;\beta)_{P=0} & (A;\alpha)_{P=5} \xrightarrow{0}_{k\ \ k+1} (B;\beta)_{P=0} \\ (A;\alpha)_{P=3} \xrightarrow{1}_{k\ \ k+1} (C;\gamma)_{P=4} & (A;\alpha)_{P=5} \xrightarrow{1}_{k\ \ k+1} (C;\gamma)_{P=4} \\ (A;\alpha)_{P=3} \xrightarrow{SB}_{k\ \ k+1} (A;\beta)_{P=0} & (A;\alpha)_{P=5} \xrightarrow{SB}_{k\ \ k+1} (A;\beta)_{P=0} \end{array} \tag{6}$$

3.4. Final state decision

The final state of the extended trellis is selected in order to minimize the overall distance between the symbol sequence and the received signal. This minimization can be done using the state variable Γ introduced in [9] (representing the distance between the symbol sequence leading to the associated state and the received signal). Moreover, the selection of the final state must ensure that the number of information bits of the message is 168 (as defined in the AIS standard) and that the final $\widetilde{\text{CRC}}$ state is zero according to (1). The number of information bits on the path ending on a given extended state can be computed with the number of received symbols at this state and a state variable S (described in [9]) representing the number of stuffing bits received on the path leading to this state.

When a final state is selected according to the previous constraints and when its state variable C is different from zero, transmission errors have not been corrected. It may not be necessary to try to extract the message from the trellis at this point.

4. SIMULATIONS

This section presents some simulation results. The proposed optimized algorithm is compared to the algorithm presented in [9]. Both implement the phase tracking strategy described in [11]. This phase tracking strategy allows the receiver to be robust to phase noise and to inaccurate modulation index h. In these simulations, the messages are generated according to the AIS recommendation: they are composed of 168 information bits concatenated with a 16-bit CRC. The stuffing bits are then inserted. The frame is encoded with NRZI, and modulated in GMSK with a bandwidth-bit-time product parameter $BT = 0.4$. The generator polynomial for CRC computation is $G(x) = x^{16} + x^{12} + x^5 + 1$. An additive white Gaussian noise (AWGN) channel is considered. In this paper, one assumes perfect carrier and timing recovery. The simulations are conducted without introducing phase noise: the implementation of phase tracking is only done to obtain a fair time processing estimation.

The proposed algorithm allows the number of CRC bits $N_{\widetilde{\text{CRC}}}$ considered for error correction to be selected between 0 and 16. This variable number of bits is useful to modulate the processing duration according to the expected performance. $N_{\widetilde{\text{CRC}}} = 0$ means that no correction is performed, $N_{\widetilde{\text{CRC}}} = 16$ gives the performance presented in [9] by using the full CRC, while $N_{\widetilde{\text{CRC}}} = 8$ yields intermediate performance with a faster computation time when compared to $N_{\widetilde{\text{CRC}}} = 16$. Table 1 presents the measured execution time on a desktop computer for different CRC lengths. Fig. 2 shows the demodulation performance in terms of packet error rate (PER). Obviously, the PER decreases when the number of CRC bits used for correction increases.

Table 1. Execution time

CRC bits	Duration
0 bit	1.2 ms
8 bits	15.3 ms
12 bits	136.4 ms
16 bits	2074.0 ms

In order to optimize the decoding performance within the allowed time period, we propose to implement an iterative receiver. Each iteration exploits more CRC bits than the previous one, until

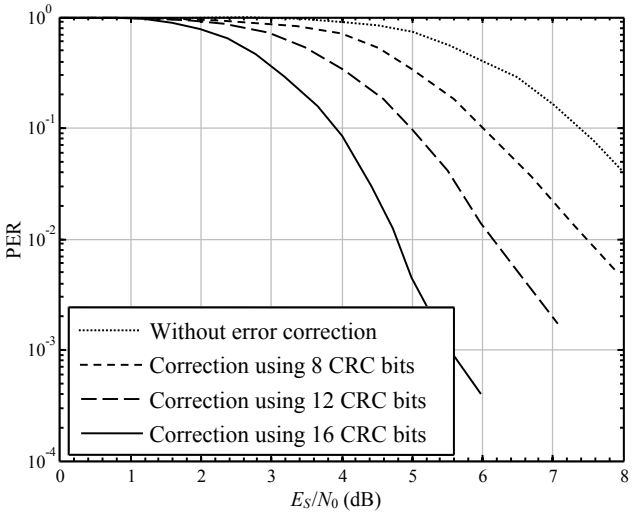

Fig. 2. PER after correction. Comparison of correction performance using 0, 8, 12 and 16 bits of the CRC.

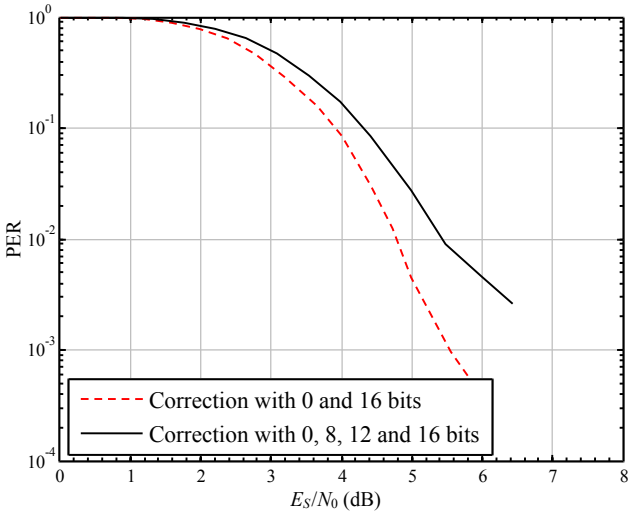

Fig. 3. PER after correction. The proposed receiver is compared with the algorithm presented in [9].

no error is detected using the remaining CRC bits. Two configurations are considered:

- The first configuration consists of two iterations only. The first iteration is achieved without error correction ($N_{\widetilde{\text{CRC}}} = 0$) and the second iteration with $N_{\widetilde{\text{CRC}}} = 16$ bits used for error correction. This configuration uses the algorithm of [9] and is presented as a reference.
- The second configuration uses different values of $N_{\widetilde{\text{CRC}}}$ for error correction. More precisely, iterations using 0, 8, 12 and 16 CRC bits are successively performed.

The PER curves for these two configurations are presented in Fig. 3. The performance of the optimized receiver (configuration 2) is slightly below that of the reference receiver (configuration 1). However, the difference is less than 0.5 dB for the target PER of 0.1 specified by the AIS standard. This performance loss is caused by undetected errors due to the limited number of CRC bits used for error detection. In view of the reduced computational cost, this performance loss is not significant and can be accepted.

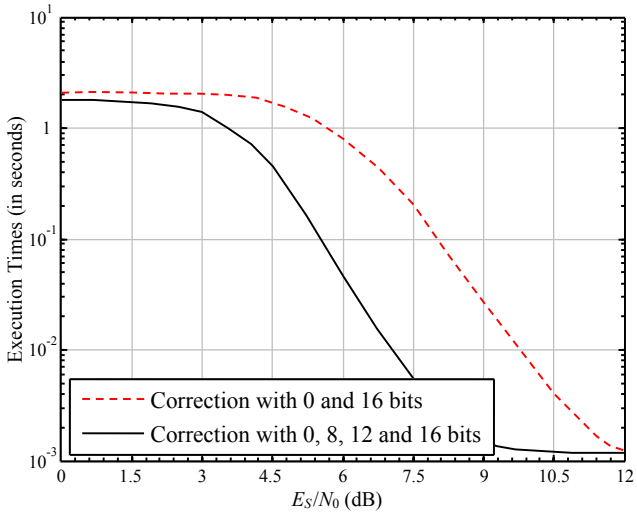

Fig. 4. Average time for decoding. The proposed receiver is compared with the algorithm presented in [9].

Fig. 4 shows the average decoding times for each configuration. Note that what matters here is the comparison between these two curves, and not the absolute value of the time measurements (which depend strongly on the computer used for simulations, here a 2.6-GHz desktop computer). One can notice that, for the considered configuration, the decoding time of the proposed receiver is in average 10 times shorter than the receiver based on the full-length CRC, when the ratio E_S/N_0 is between 5 and 10 dB (which is usual for AIS signals received by satellite).

5. CONCLUSION

This paper presented a new demodulation algorithm for AIS signals received by a satellite. The main advantage of this algorithm is its complexity which has been optimized by considering only portions of the CRC for error correction purposes. Using an extended trellis allows one to use the CRC included in the messages to correct transmission errors. The optimized version presented in this paper provided execution times divided by a factor 10 when compared to the receiver using the full-length CRC, with a negligible impact on the decoding performance. Future works will focus on the optimal selection of $N_{\widetilde{\text{CRC}}}$ of the iterations that minimizes the execution times of the algorithm, while maintaining low difference in performance compared to the full-CRC case.

6. RELATION TO PRIOR WORK

The reception of AIS signals by satellite is a very active subject [3–8] which led us to propose new transmission error correction methods [9, 14]. This paper is proposing a way of reducing the computational time of the algorithm of [9, 14] by considering a CRC with reduced length. The performance of the resulting demodulation decoding algorithm is shown to be very promising.

7. REFERENCES

[1] Recommendation ITU-R M.1371, "Technical characteristics for a universal automatic identification system using time division multiple access in the VHF maritime mobile band." ITU, 2001.

[2] "exactEarth," *http://www.exactearth.com*, 2010.

[3] A. Scorzolini, V. D. Perini, E. Razzano, G. Colavolpe, S. Mendes, P. Fiori, and A. Sorbo, "European enhanced space-based AIS system study," in *Proc. Adv. Sat. Mul. Sys. Conf.*, no. 5, Cagliari, Italy, Sept. 2010, pp. 9–16.

[4] M. J. Gallardo and U. Sorger, "Coherent receiver for AIS satellite detection," in *Int. Symp. Commun. Control Signal Process.*, vol. 4, Limassol, Cyprus, Mar. 2010, pp. 1–4.

[5] J. Larsen, H. Mortensen, and J. Nielsen, "An SDR based AIS receiver for satellites," in *Proc. Int. Conf. Recent Advances in Space Technologies*, vol. 5, Istanbul, Turkey, June 2011, pp. 526–531.

[6] M. Zhou, A. van der Veen, and R. van Leuken, "Multi-user LEO-satellite receiver for robust space detection of AIS messages," in *Proc. IEEE Int. Conf. Acoust., Speech, and Signal Processing*, vol. 37, Kyoto, Japan, Mar. 2012, pp. 2529–2532.

[7] N. Bouny, J. LeMaitre, and J.-P. Millerioux, "Results of measurement campaign for characterisation of AIS transmitters," in *Proc. Adv. Sat. Mul. Sys. Conf.*, vol. 12, Baiona, Spain, Sept. 2012, pp. 258–265.

[8] M. Picard, M. R. Oularbi, G. Flandin, and S. Houcke, "An adaptive multi-user multi-antenna receiver for satellite-based AIS detection," in *Proc. Adv. Sat. Mul. Sys. Conf.*, vol. 12, Baiona, Spain, Sept. 2012, pp. 273–280.

[9] R. Prévost, M. Coulon, D. Bonacci, J. LeMaitre, J.-P. Millerioux, and J.-Y. Tourneret, "CRC-assisted error correction in a trellis coded system with bit stuffing," in *Proc. IEEE Workshop on Stat. Signal Process.*, Nice, France, June 2011, pp. 381–385.

[10] R. Prévost, D. Bonacci, M. Coulon, J. LeMaitre, J.-P. Millerioux, and J.-Y. Tourneret, "Interference mitigation and error correction method for AIS signals received by satellite," in *Proc. European Signal and Image Processing Conf.*, Bucharest, Romania, Aug. 2012, pp. 46–50.

[11] ——, "Joint phase-recovery and demodulation-decoding of AIS signals received by satellite," in *Proc. IEEE Int. Conf. Acoust., Speech, and Signal Processing*, Vancouver, Canada, May 2013, pp. 4913–4917.

[12] ——, "Multi-encodage error correction with extended trellis," Patent Pending.

[13] ——, "A Viterbi algorithm with conditional transitions," Patent Pending.

[14] ——, "Extended constrained Viterbi algorithm for AIS signals received by satellite," in *Proc. IEEE-AESS Conf. Telecom. Satellite*, Rome, Italy, Oct. 2012.