JITTER REQUIREMENTS FOR BANDPASS SAMPLING RECEIVERS UTILIZING SAMPLE-AND-HOLD CIRCUITS

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ABSTRACT

The uncertainty of the sampling time is of major concern for bandpass signal reception. It reduces the achievable signal-to-noise ratio of the bandpass sampling receiver. Traditionally, only the absolute sampling time is considered to be subject to timing errors, which then result in corresponding amplitude errors. But jitter also has an impact on the integration duration of the sample-and-hold circuit. In this paper we investigate the impact of jitter on the signal-to-noise ratio performance of the bandpass sampling receiver utilizing a sample-and-hold sampling circuit. In addition, a bound on the acceptable standard deviation of the jitter for different receiver setups is given.

Index Terms— ADC, jitter, SNR, bandpass sampling, sample-and-hold circuit

1. INTRODUCTION

Utilizing a bandpass sampling receiver reduces the amount of analog components, digitizes the received bandpass signal, and hence allows digital processing at an early stage [1]. Still, there are several drawbacks of this architecture which degrade the system performance, i.e. noise folding, which reduces the signal-to-noise ratio (SNR). A key component in the overall receive chain is the analog-to-digital converter (ADC). Especially, the effect of sampling time uncertainty has to be considered carefully given that the received bandpass (BP) signals are located at carrier frequencies in the gigahertz range

The problem of time uncertainty, or jitter, in sampling was introduced in [2], first. Since [3], jitter is typically categorized into three types: 1) input signal jitter, 2) sampling circuit jitter, and 3) sampling clock jitter. The mapping from the latter two timing errors to the associated amplitude errors is commonly based on a Taylor series expansion [3]. The impact of uncorrelated realizations of the jitter, arising from the clock and the sampling circuit, on the SNR was studied and validated by providing a general model for the sample-and-hold (SH), also known as charge sampling (CS) circuit, in [4, 5]. An analytical model based on the root mean square (RMS) jitter was presented by [6]. It validates the results from [4]. In [7], the former analysis was then extended to a detailed model of the time domain error signal and the spectral shaping of the jitter for BP sampling.

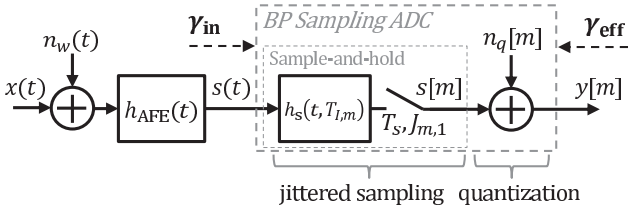

Fig. 1. System model of the bandpass sampling ADC.

In this paper, we investigate the effect of jitter on the characteristics of the SH circuit. Moreover, we show the influence of jitter on the effective in-band SNR performance of the BP ADC (Sec. 2), and identify the most harmful type of jitter (Sec. 3) as well as the maximum acceptable standard deviation of the jitter for given application scenarios (Sec. 4). The model of the BP ADC, depicted in Fig. 1, incorporates the characteristics of the analog frontend (AFE) $h_{\text{AFE}}(t)$, the SH circuit as the main part of this analysis, and the quantization stage with a limited resolution of b bit. The SH circuit, which is dependent on the actual realization of the jitter, is modeled as a combination of a linear filter with impulse response $h_{\text{s}}\left(t, T_{I,m}\right)$, and an ideal sampler with sampling period T_s and an absolute sampling time error $J_{m,1}$. The used input signals $s(t)$ are characterized by their rectangular shaped power spectral densities (PSD) centered at the carrier frequency f_c and with a bandwidth of $B = 2f_g$. The effective in-band SNR at input and the output of the ADC is denoted as γ_{in} and γ_{eff}, respectively.

2. SYSTEM MODEL

The BP ADC, shown in Fig. 1, is separated in two parts: the sampling stage, and the quantization.

The *sampling stage* models the characteristics of the SH circuit as a concatenation of a linear impulse response $h_{\text{s}}\left(t, T_{I,m}\right)$, and an ideal sampling switch operating at rate $f_s = 1/T_s$ with time error $J_{m,1}$. This model is equivalent to the commonly used approach of integrating the input signal:

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$$s[m] = \int_{mT_s+J_{m,1}}^{(m+d)T_s+J_{m,2}} s(t)\,\mathrm{d}t. \tag{1}$$

We denote $d \in (0,1]$ as the duty cycle, and the product $d \cdot T_s$ is called the integration time T_I. For the case of jitter, the upper and lower limit of the integral is shifted by an additive term $J_{m,1}$ and $J_{m,2}$, respectively. We can now distinct two influences of the jitter: the jitter of the absolute sampling time $t_m = mT_s + J_{m,1}$, and the jitter of the integration duration $T_{I,m}$ of the m-th sample. Both influences are also shown in Fig. 2.

We define the absolute sampling time jitter to be $J_{m,1}$. The length of the integration interval in sample mode for the m-th sample is determined by

$$T_{I,m} = d \cdot T_s + J_{m,2} - J_{m,1} = T_I + \Delta J_m > 0 \;\forall m \in \mathbb{Z}. \tag{2}$$

The integration of a input signal for the duration of $T_{I,m}$ as in (1) corresponds to a convolution with a moving, rectangular shaped, window with the same width $T_{I,m}$. This allows us to formulate the general normalized transfer function of the SH circuit impaired by time jitter as

$$H_\mathrm{s}(f, T_{I,m}) = \sqrt{T_{I,m}} \cdot \mathrm{sinc}\left(f \cdot T_{I,m}\right). \tag{3}$$

Here, $\mathrm{sinc}(x) = \sin(\pi x)/\pi x$. To model the relation between the input SNR and the output SNR of the SH we propose a two step approach. First, we formulate the impact of integration time jitter on the SNR after linear filtering with $H_\mathrm{s}(f, T_{I,m})$. Then, we take the impact of absolute timing errors $J_{m,1}$ for ideal sampler into account.

The characteristics of the transfer function of the sampling circuit are assumed to be described by (3). For the evaluations, we consider the second order moments of the desired input signal and the noise. The signals are described by their PSDs $S_{xx}(f)$ and $S_{nn}(f)$, respectively. With this, the signal-to-sampling-noise ratio (SSNR) is formulated as

$$\gamma_s\left(T_{I,m}\right) = \frac{\int_0^\infty S_{xx}(f)|H_\mathrm{s}(f, T_{I,m})|^2\,\mathrm{d}f}{\sum_i \int_0^\infty S_{nn}(f - if_\mathrm{s})|H_\mathrm{s}(f, T_{I,m})|^2\,\mathrm{d}f}. \tag{4}$$

The absolute sampling time error is incorporated by applying a first-order Taylor expansion [3] to transfer the time shift $J_{m,1}$ into an amplitude shift Δs_m.

$$s\left(mT_s + J_{m,1}\right) \approx s(mT_s) + J_{m,1}\left.\frac{\mathrm{d}s(t)}{\mathrm{d}t}\right|_{t=mT_s} \tag{5}$$

This allows to approximate the signal-to-jitter-noise ratio (SJNR) for narrow-band BP signals with a cut-off frequency f_g, a carrier frequency f_c and a jitter variance σ_j^2 (cp. [3]) as

$$\gamma_j\left(f_c, \sigma_j\right) \approx \left(4\pi^2 f_c^2 \sigma_j^2\right)^{-1} \quad \text{if} \quad \frac{f_g}{f_c} \ll 1 \wedge f_c \ll \sigma_j^{-1}. \tag{6}$$

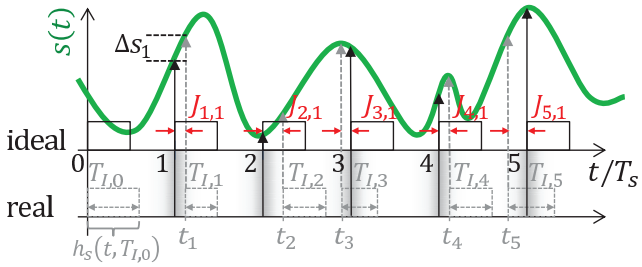

Fig. 2. Ideal timing and real timing of a SH circuit including the effects of the absolute time errors $J_{m,1}$ and the time-varying integration duration $T_{I,m}$.

In the second stage of the BP ADC, the impact due to *quantization* of the sampled signal is formulated by the signal-to-quantization-noise ratio (SQNR). Assuming an uniformly distributed quantization error, it can be formulated as (cp. [8])

$$\gamma_\mathrm{q}\left(b, \beta, \eta\right) = 3 \cdot 4^b \cdot \frac{\beta}{\eta}. \tag{7}$$

It is a function of the resolution of b bit, the oversampling ratio (OSR) $\beta = f_s/(2B)$, and the peak-to-average-power ratio (PAPR) η.

Finally, the input-output relation of the SNR for the band-pass sampling ADC in Fig.1 is determined by combining the three separate SNRs from (4), (6), and (7) to

$$\gamma_\mathrm{eff} = \frac{\gamma_\mathrm{q}\gamma_\mathrm{j}\gamma_\mathrm{s}}{\left(\gamma_\mathrm{q}+1\right)\left(\gamma_\mathrm{j}+\gamma_\mathrm{s}+1\right)+\gamma_\mathrm{j}\gamma_\mathrm{s}}. \tag{8}$$

This allows the evaluation of the effective in-band SNR utilizing a SH circuit. Furthermore, it is used to study the acceptable jitter for predefined SNR requirements.

3. HOW JITTER IMPACTS THE SAMPLE-AND-HOLD CIRCUIT

The previous section described how jitter generally affect the SH performance in terms of absolute timing error $J_{m,1}$ and time-varying integration time $T_{I,m}$. In a practical system, two types of jitter sources are commonly distinguished (cp. [3]). First, sampling circuit jitter, or aperture jitter, originating from circuit noise and modeled as an i.i.d. Gaussian distributed error with zero-mean and variance σ_ap^2. Second, the clock jitter modeled as a Wiener process (cp. [9]) with zero-mean and linearly increasing variance $\sigma_{\mathrm{clk},m}^2 = mcT_s$. Here, m is the discrete sample index, c is an oscillator constant characterizing the quality of the signal, and T_s is the sampling period. Both stochastic processes are considered to be mutually independent, and both will have an influence on the absolute timing error and the integration time.

After the general derivations in the previous section, we will now investigate the influence on the received signal quality under the assumptions given above. For this, the term ΔJ_m from (2) is reformulated as a function of the aperture

and clock jitter:

$$\Delta J_m = J_{m,2} - J_{m,1} = \underbrace{J^{(\text{ap})}_{m,2} - J^{(\text{ap})}_{m,1}}_{\text{aperture jitter}} + \underbrace{J^{(\text{clk})}_{m,2} - J^{(\text{clk})}_{m,1}}_{\text{clock jitter}}. \quad (9)$$

This resulting process still has zero-mean and the variance $\sigma^2_{\Delta j}$ is obtained by

$$\begin{aligned}\sigma^2_{\Delta j} &= E\left[(\Delta J_m)^2\right] \\ &= 2\sigma^2_{\text{ap}} + \sigma^2_{\text{clk},2} + \sigma^2_{\text{clk},1} - 2E\left[J^{(\text{clk})}_{m,2} J^{(\text{clk})}_{m,1}\right] \\ &= 2\sigma^2_{\text{ap}} + \sigma^2_{\text{clk},2} + \sigma^2_{\text{clk},1} - 2E\left[\left(J^{(\text{clk})}_{m,1} + \delta_m\right) J^{(\text{clk})}_{m,1}\right] \\ &= 2\sigma^2_{\text{ap}} + \sigma^2_{\text{clk},2} - \sigma^2_{\text{clk},1} = 2\sigma^2_{\text{ap}} + d \cdot cT_s. \quad (10)\end{aligned}$$

Here, δ_m describes the change in the clock jitter $J_{m,2} = J_{m,1} + \delta_m$. Given an i.i.d. Gaussian aperture jitter process and a Wiener clock jitter process with i.i.d. Gaussian increments, the variance $\sigma^2_{\Delta j}$ is a sum of twice the aperture jitter variance, and the variance $d \cdot cT_s$. The resulting variance is independent from the sample index m. The contribution of the aperture jitter is doubled due to assumption of independent realizations at opening and closing time of the sampling switch. For clock jitter, only the change of the variance during the duty cycle d is of interest.

Eq. (10) is simplified further by using practical constraints for both types of jitter. A lower bound on practical achievable values for the aperture jitter is set to $\sigma_{\text{ap}} = 0.1$ ps (cp. [10]). For the clock jitter, the oscillator constant is typically in the range $c \in [10^{-23}, 10^{-19}]$ s, and the sampling period is about $T_s \geq 10^{-9}$ s ($f_s \leq 1$ GHz). It turns out, that the impact of the aperture jitter on the variance $\sigma^2_{\Delta j}$ is orders of magnitude larger than impact of the clock jitter. Hence, (10) is mainly determined by the effect of aperture jitter and we can describe the time-varying integration time $T_{I,m}$ approximated by

$$T_{I,m} \approx dT_s + J^{(\text{ap})^*}_m = dT_s + J^{(\text{ap})}_{m,2} - J^{(\text{ap})}_{m,1} > 0 \quad \forall m \in \mathbb{Z} \quad (11)$$

with $J^{(\text{ap})^*} \sim \mathcal{N}\left(0, 2\sigma^2_{\text{ap}}\right)$.

With this result, we can now evaluate the impact of aperture jitter on the spectral shape $H_{\text{s}}(f, T_{I,m})$ from (3) of the SH circuit. Especially in BP sampling applications, where the sampling rate is smaller then the carrier frequency $f_s < f_c$, the signal has to be positioned not to be in a notch of the SH transfer function. Otherwise the desired signal experience a strong attenuation. Conversely, this can be useful in case of attenuating strong interfering signals. Another considerable scenario is multi-band signal reception. Given two signals, located at two non-contiguous frequency bands, shall be received in parallel. For this case, the sampling circuit has to designed such that both bands are not suppressed by the filter.

The notches of (3) are located at the notch frequencies $f_{\text{notch,m}} = \pm k/T_{I,m}$. Given the assumption of $\sigma_{\text{ap}} = 0.1$ ps, duty cycle of $d = 0.5$, and sampling period of $T_s = 10^{-9}$ s, the ratio of aperture jitter to integration time is $\sqrt{2}\sigma_{\text{ap}}/dT_s \approx 0.03\%$. If the desired signal band is positioned such that it is not in a notch of (3), we do not see an impact of jitter on the SNR performance in bandpass sampling applications. Hence, we can assume the transfer function to be independent from jitter: $H_{\text{s}}(f, T_{I,m}) \approx H_{\text{s}}(f, dT_s)$. In conclusion, the absolute sampling time error $J_{m,1}$ is more crucial to the overall system performance in BP sampling then the time-varying integration time $T_{I,m}$.

4. JITTER REQUIREMENTS

To apply a bandpass sampling receiver in a realistic scenario, its has to be configured such that the performance degradation in terms of ADC noise figure α is limited to a certain maximum value. Within this paper, the metric of the effective in-band SNR γ_{eff} is used to obtain an input-output relation on the signal quality such that

$$\gamma_{\text{eff}} = \frac{\gamma_{\text{in}}}{\alpha}. \quad (12)$$

On the one hand, this equation can be used to determine the effective in-band SNR at each stage of the receiver as a function of the input SNR γ_{in}. On the other hand, we can apply it to evaluate the required standard deviation of the jitter for a given receiver configuration with a sampling rate f_s, a duty cycle d, a resolution b, and a specific performance requirement α. The ADC noise figure α is defined as

$$\alpha = \frac{(\gamma_{\text{q}} + 1)\left((\gamma_{\text{j}} + 1)\,\alpha_s + \gamma_{\text{in}}\right) + \gamma_{\text{j}}\gamma_{\text{in}}}{\gamma_{\text{q}}\gamma_{\text{j}}}, \quad (13)$$

using (12), (8) and the relation $\gamma_{\text{s}} = \gamma_{\text{in}}/\alpha_s$. The term α_s is numerically evaluated based on (4) for the given input signal with carrier frequency f_c and bandwidth B. It describes the noise figure of the SH circuit. Further, using (6) and (7) leads to an analytically formulation of the jitter standard deviation:

$$\sigma_j \leq \frac{1}{2\pi f_c}\sqrt{\frac{3 \cdot 4^b \frac{\beta}{\eta}\alpha - \alpha_s\left(1 + 3 \cdot 4^b \frac{\beta}{\eta}\right) - \gamma_{\text{in}}}{(\alpha_s + \gamma_{\text{in}})\left(1 + 3 \cdot 4^b \frac{\beta}{\eta}\right)}}. \quad (14)$$

It is obvious that the maximum allowed standard deviation of the jitter is inversely proportional to carrier frequency f_c of the sampled signal.

Now let us consider the example depicted in Fig. 3. It shows the usage of the proposed approach to evaluate the jitter requirements for the BP ADC. The considered ADC noise figure is set to 5 dB or 10 dB, respectively. The dashed horizontal gives a lower bound on the aperture jitter of current ADCs of 0.1 ps [10]. For the case of 6 bit of quantization resolution, there are three distinguishable regions depending on the SNR γ_{in} of the input signal.

For low input SNR up to ≈ 41.9 dB, which corresponds to the SQNR from (7) for $b = 6$ bit, $\beta = 20$, and $\eta = 12$ dB of a multi-carrier signal, the jitter requirements increases inversely

proportional to carrier frequency f_c. In this part, the jitter requirement is chosen such that the effective in-band SNR performance of the receiver still mets the required noise figure α. It follows a transitional area, where jitter and quantization errors are both contributing. If the input SNR is further increased, the BP ADC is not able to fulfill the requirements of the ADC noise figure α due to its limited resolution. In this case, further improvements on the jitter values will also have no effect on the SNR. Hence, the resolution b has to be increased for a scenario with higher input SNR.

It has to be taken into consideration that jitter errors are not always the reason for the limited SNR performance of the BP ADC. Especially the SH sampling circuit limits the SNR of the signal. If the SSNR is already less then the calculated SJNR, jitter will not affect the system performance.

5. CONCLUSIONS

In this paper the impact of time jitter on bandpass sampling receivers using a sample-and-hold circuit has been evaluated. For this, the relation between in-band input SNR and the effective in-band SNR at the output of the BP ADC is analyzed. The investigations emphasize on the impact of the two prominent types of jitter on the SNR performance. First, the effect of a varying integration time of the SH circuit, and second, the effect of errors in the absolute sampling time. It turns out that the SNR is more prone to absolute sampling time errors as to the varying integration time in bandpass sampling application scenarios. This means that the duration of impulse function of the SH circuit can be considered to be jitter independent.

Furthermore, we evaluated the maximum acceptable standard deviation of the jitter for the BP ADC for two different assumptions on the ADC noise figure α and quantization resolution b. It is shown that the jitter requirements are dependent on the receiver configurations and the characteristics of the received signal. The required jitter values decrease proportionally with the target SNR of the receiver. In addition, the presented ideas are also useful to assess the gain of digital estimation and compensation algorithms.

6. ACKNOWLEDGMENT

This work is supported in a part by the German Research Foundation (DFG) in the Collaborative Research Center 912 "Highly Adaptive Energy-Efficient Computing".

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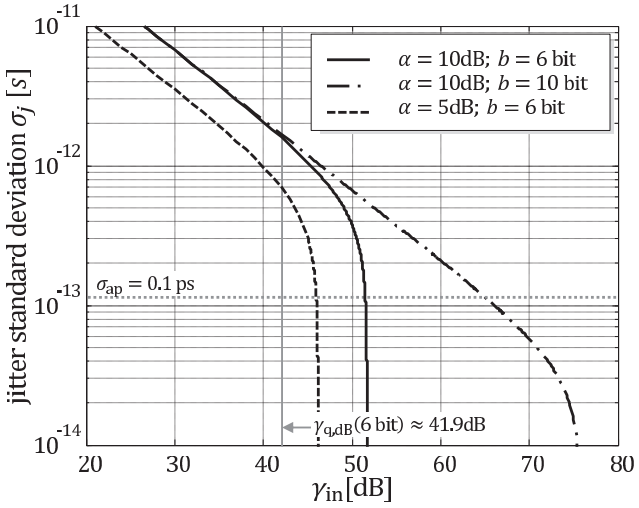

Fig. 3. Required standard deviation σ_j of the jitter for the BP ADC with a noise figure of $\alpha = 5, 10$ dB, a quantization resolutions of $6, 10$ bit, and a noise figure of $\alpha_s = 3$ dB for the SH circuit as a function of the SNR γ_{in} of the input signal $s(t)$. The considered input signal has a carrier frequency of $f_c = 2.31$ GHz and bandwidth $B = 20$ MHz. The sampling rate is $f_s = 800$ MHz.

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