DIGITAL BACKGROUND CALIBRATION FOR PIPELINED ADCS

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ABSTRACT

Pipelined ADCs with more than 12 bits of resolution typically require linearity enhancement. This paper shows that the gain errors of both the sub DACs and interstage amplifiers in a pipelined ADC can be digitally corrected. A background calibration method is developed employing an energy free methodology for both single and multi stage errors and simulation results are presented to demonstrate the effectiveness of the proposed method.

Index Terms— pipelined ADCs, interstage gain, background calibration, energy free

1. INTRODUCTION

The continuous scaling of CMOS technology has led to improvements in the performance of digital circuits and allowed for the integration of complex digital algorithms on chip. Digitally enhanced analog design attempts to leverage digital correction and calibration techniques to improve analog performance [1]. One example is digital calibration in a pipelined ADC to improve the resolution when it is limited by interstage gain errors resulting from capacitor mismatches and finite op amp gains [2]. Trimming is one method of digital calibration, however, it cannot track variations over time due to temperature and power supply changes. As such, background calibration methods which continually adapt are common to include.

This paper proposes to correct interstage gain errors using an energy free background calibration method. Energy free methods use a small amount of oversampling to provide the degrees of freedom necessary for blind identification [9], [10]. Positive aspects of this application of the the energy free method include fast convergence, no reduction in the full scale signal amplitude and the ability to simultaneously correct multiple interstage gain errors.

2. RELATION TO PRIOR WORK

There are a number of methods for background calibration of pipelined ADCs. For example, [3] uses a skip and fill algorithm in which a conversion sample is occasionally skipped and a sample of a calibration signal is converted and used to perform interstage gain estimation. The missing input sample is later generated using a nonlinear interpolation filter. A similar queue based calibration scheme was proposed in [4] for algorithmic ADC designs.

Other background calibration methods inject a known PN modulated dither signal into the gain path to measure the interstage gain error and later subtract it digitally [5] - [8]. The dither signal needs to be small such that the signal plus dither does not exceed the full scale range of the sub DAC. However, it is difficult to detect a small PN modulated dither signal in the presence of a large uncorrelated signal. Thus, dither based calibration methods typically require a large number of samples to converge.

3. SINGLE INTERSTAGE GAIN CALIBRATION

A pipelined ADC consists of $N+1$ stages and N interstage amplifiers where interstage gain errors create nonlinear distortion. This section focuses on the calibration of the 1st interstage gain and thus uses a 2 stage system (Fig. 1) where the 2nd stage (or backend) sub ADC represents the combined effects of all remaining ADC stages.

3.1. Optimal digital gain

As shown in Fig. 1, D_1, D_2 and D are the output of the 1st stage, 2nd stage and entire pipelined ADC, respectively. G_{D1} is the digital combination gain and the ADC output is expressed as

$$D = D_1 + \frac{1}{G_{D1}} D_2. \tag{1}$$

Modeling the sub ADCs as adding quantization noise and the sub DAC as a linear gain, (1) can be rewritten as

$$D = \left[1+(1-G_{A1})\frac{G_1}{G_{D1}}\right]V_{in} + \left(1-\frac{G_{A1}G_1}{G_{D1}}\right)q_1 + \frac{q_2}{G_{D1}}, \tag{2}$$

where V_{in} is the ADC analog input, q_1 and q_2 are the quantization noise of the 1st stage and back end sub ADCs and G_1 and G_{A1} are the gains of interstage amplifier and sub DAC.

Ideally, the interstage amplifier and sub DAC are gain error free, i.e., $G_{A1} = 1$, $G_1 = G_{1,\text{ideal}}$. $G_{1,\text{ideal}}$ depends

on the resolution of the sub ADC and it is common to set $G_{1,\text{ideal}} = 2^{b_1-1}$ where b_1 is the number of bits in the 1st stage sub ADC. The digital gain is set to be the same as interstage gain $G_{D1} = G_{1,\text{ideal}}$. With these choices (2) reduces to

$$D = V_{in} + \frac{1}{G_{1,\text{ideal}}} q_2, \tag{3}$$

which implies that the overall quantization error of the ADC is given by the the back end ADC quantization error q_2 scaled by the gain of the 1st stage.

However, when the interstage power amplifier gain G_1 or sub DAC gain G_{A1} is subject to a linear error, e.g., $G_1 = G_{1,\text{ideal}} + \epsilon$, the 1st stage quantization noise q_1 cannot be completely cancelled and nonlinear distortion is introduced.

From (2), the necessary and sufficient condition to completely remove 1st stage quantization noise is

$$G_{D1} = G_1 G_{A1}. \tag{4}$$

This implies that the gain error in the analog circuit (either G_1 or G_{A1}) can be compensated by adjusting G_{D1} in the digital domain such that (4) holds. The calibrated ADC output is obtained by substituting (4) into (2)

$$D = \left[1 + \frac{1 - G_{A1}}{G_{A1}}\right] V_{in} + \frac{1}{G_1 G_{A1}} q_2. \tag{5}$$

Comparing (3) and (5), the calibrated output is a scaled version of the ideal output, which has negligible impact in most of applications.

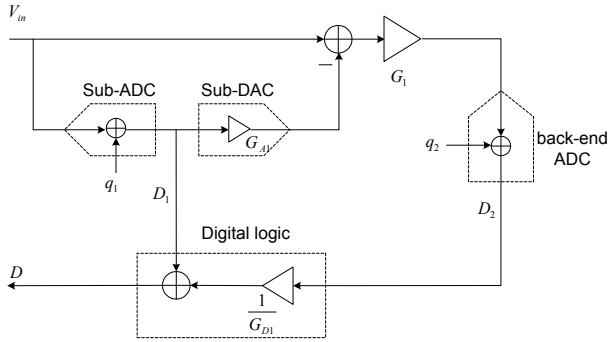

Fig. 1. A 2 stage pipelined ADC.

3.2. Proposed calibration method

To satisfy (4) the digital gain G_{D1} is estimated as

$$\hat{G}_{D1} = \arg \min_{G_{D1}} J(G_{D1}), \tag{6}$$

where

$$J(G_{D1}) = E\left[(G_{D1} - G_1 G_{A1})^2\right]. \tag{7}$$

The signed LMS algorithm results in the recursive estimate

$$\hat{G}_{D1}(k+1) = \hat{G}_{D1}(k) - \mu \cdot \text{sgn}\left[\nabla J_{G_{D1}}(k)\right], \tag{8}$$

where μ is the step size, sgn$[\cdot]$ denotes the sign function and the instantaneous gradient is

$$\nabla J_{G_{D1}}(k) = 2\left(\hat{G}_{D1}(k) - G_1 G_{A1}\right). \tag{9}$$

Note that $\nabla J_{G_{D1}}(k)$ is not available since both G_1 and G_{A1} are unknown.

Similar to [9] and [10] it is assumed that the input signal V_{in} is slightly oversampled and there is no signal energy in the high frequency region. This high frequency region will be referred to as the energy free band.

Due to errors in G_1 and G_{A1}, the q_1 component in the ADC output creates energy in the energy free band. Passing the ADC output through the high pass filter f_{HP} with a cut off frequency equivalent to the input signal bandwidth results in

$$\tilde{D} = D * f_{HP} = \left(1 - \frac{G_{A1} G_1}{G_{D1}}\right) \tilde{q}_1 + \frac{1}{G_{D1}} \tilde{q}_2, \tag{10}$$

where $*$ denotes linear convolution and $\tilde{q}_1$ and $\tilde{q}_2$ are high pass versions of q_1 and q_2, respectively

$$\tilde{q}_1 = q_1 * f_{HP} \quad \text{and} \quad \tilde{q}_2 = q_2 * f_{HP}. \tag{11}$$

Note that no component of the input V_{in} exists in (10) because V_{in} has no energy in the energy free region.

Define $\tilde{D}_2$ as the high pass version of the 2nd stage output

$$\tilde{D}_2 = D_2 * f_{HP}. \tag{12}$$

Since q_2 and D_2 are uncorrelated, correlating $\tilde{D}_2$ with both sides of (10) leads to

$$E[\tilde{D}\tilde{D}_2] = \left(1 - \frac{G_{A1} G_1}{G_{D1}}\right) E[\tilde{q}_1 \tilde{D}_2], \tag{13}$$

where $E[\cdot]$ denotes statistical expectation. Because D_2 is the quantized version of q_1, $E[\tilde{q}_1 \tilde{D}_2] > 0$.

Combining (9) and (13) yields

$$\text{sgn}\left[\nabla J_{G_{D1}}\right] = \text{sgn}\left\{E[\tilde{D}\tilde{D}_2]\right\} \tag{14}$$

Since both $\tilde{D}$ and $\tilde{D}_2$ are available, $E[\tilde{D}\tilde{D}_2]$ can be estimated in a straightforward manner using a block of data

$$\hat{E}[\tilde{D}\tilde{D}_2] = \frac{1}{L} \sum_{l=0}^{L-1} \tilde{D}(kL + l) \tilde{D}_2(kL + l), \tag{15}$$

where L is the block size.

4. MULTIPLE INTERSTAGE GAIN CALIBRATION

In this section the proposed single stage calibration method is extended to multiple stages. For a $N+1$-stage pipelined ADC, N interstage gains ($G_i,\ i=1,...,N$) need to be calibrated. As shown in Fig. 2, $q_i, i=1,...,N+1$ denotes the quantization noise in each stage and $G_{Di}, i=1,...,N$ and $G_{Ai}, i=1,...,N$ are the digital combination gain and sub DAC gain in each stage, respectively. Errors in G_i and G_{Ai} can be simultaneously compensated by calibrating $G_{Di}, i=1,...,N$ in the digital domain.

Following the same strategy used to obtain (10), the high pass ADC output is

$$\tilde{D} = e_1\tilde{q}_1 + e_2\tilde{q}_2 + \cdots + e_N\tilde{q}_N + \tilde{q}_{N+1}, \qquad (16)$$

where $\tilde{q}_i$ is the high pass quantization noise

$$\tilde{q}_i = q_i * f_{HP},\ i=1,...,N+1, \qquad (17)$$

and e_i is a quantity depending on the interstage gain, sub DAC gain and digital combination gain of both the current and subsequent stages. Note that an explicit expression of e_i is not required for the gain calibration.

The objective of the calibration is to cancel the quantization noise up to the Nth stage, i.e., to make $e_i = 0$, by adjusting $G_{Di}, i=1,...,N$. All of the G_{Di}'s can be estimated using the signed LMS algorithm

$$\hat{G}_{Di}(k+1) = \hat{G}_{Di}(k) - \frac{\mu}{L}\mathrm{sgn}\left[\nabla J_{G_{Di}}(k)\right], \qquad (18)$$

for $i=1,...,N$.

Again, using the same strategy as the single interstage gain case, the sign of gradient is

$$\mathrm{sgn}\left[\nabla J_{G_{Di}}\right] = \mathrm{sgn}\left[e_i\right] = \mathrm{sgn}\left\{E[\tilde{D}\tilde{D}_{i+1}]\right\}, \qquad (19)$$

and the estimate for the kth block is calculated as

$$E[\tilde{D}\tilde{D}_{i+1}] = \frac{1}{L}\sum_{l=0}^{L-1}\tilde{D}(kL+l)\tilde{D}_{i+1}(kL+l). \qquad (20)$$

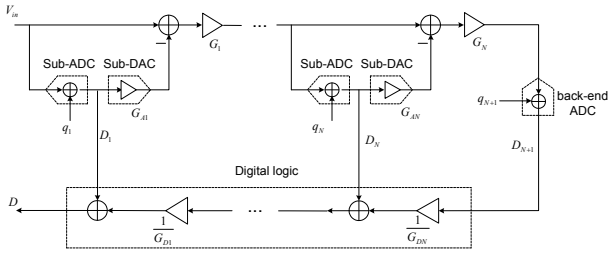

Fig. 2. A $(N+1)$ stage pipelined ADC.

5. SIMULATION RESULTS

A 4 stage 16 bit pipelined ADC was simulated. The 1st and 2nd stages have gains (with errors) $G_1 = 16.1622$ and $G_2 = 8.0639$ which deviate from their nominal values of $G_{1,\text{ideal}} = 16$ and $G_{2,\text{ideal}} = 8$. Both of the sub DACs are gain error free, i.e., $G_{A1} = G_{A2} = 1$, and the signal is oversampled by a ratio of 1.5.

To demonstrate the convergence of the proposed methods, the normalized gain estimation error is defined for each stage in each iteration as

$$E_{Di}(k) = \frac{\hat{G}_{Di}(k) - G_{Di}}{G_{Di}},\ i=1,2, \qquad (21)$$

and is shown in Fig. 3 to converge quickly. The ideal and converged digital combination gains are also shown in Table 5.

The SFDR and INL before and after calibration are depicted in Fig. 4 and Fig. 5. It is observed that the SFDR is improved from 74 dB to 128 dB and the INL is reduced to within 1 LSB.

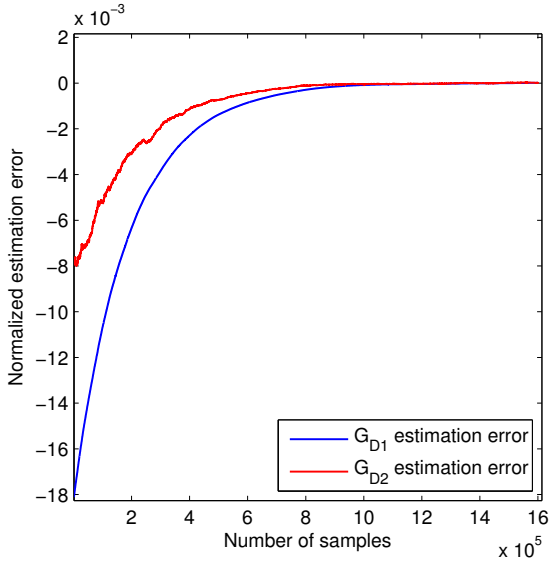

Fig. 3. Convergence of multiple digital gain estimation.

Compensation	Digital	
	G_{D1}	G_{D2}
Ideal	16.1622	8.0639
Estimate	16.1624	8.0641

Table 1. ADC interstage gain calibration results.

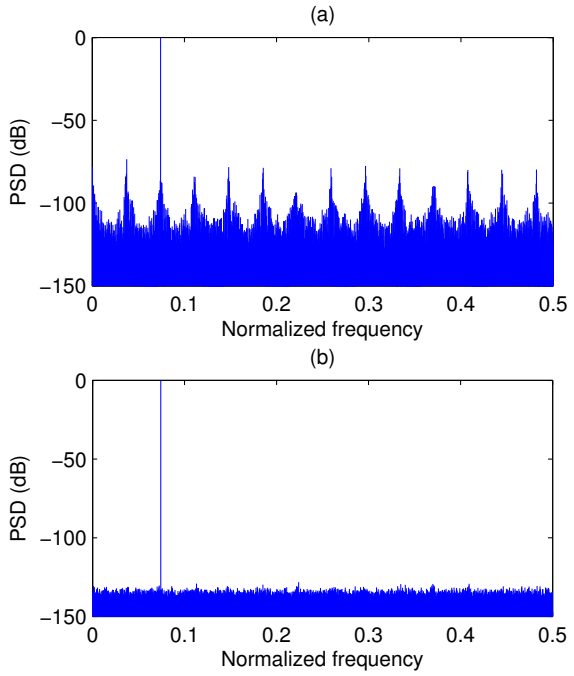

Fig. 4. SFDR (a) without calibration and (b) with calibration.

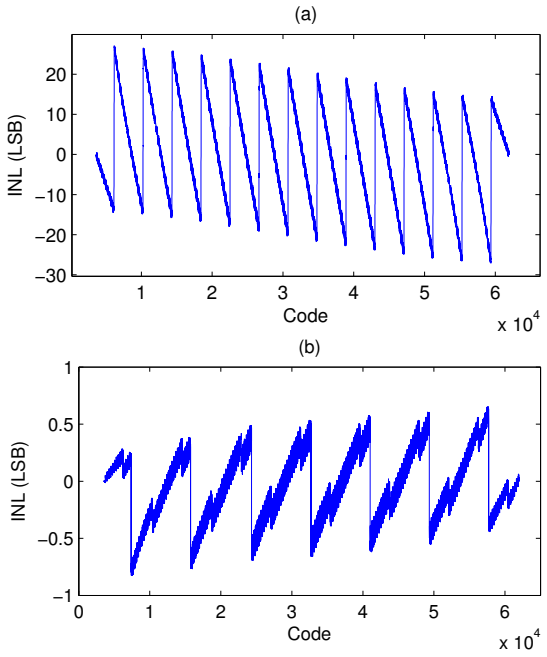

Fig. 5. INL (a) without calibration and (b) with calibration.

6. CONCLUSIONS

An adaptive background calibration algorithm based on an energy free method for correcting the linear gain errors of pipelined ADCs was presented. The technique achieves fast convergence at the cost of oversampling.

7. REFERENCES

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