ADAPTIVE FILTER BASED LOW COMPLEXITY DIGITAL INTENSIVE HARMONIC REJECTION FOR SDR RECEIVER

Chunshu Li, Min Li, Marian Verhelst,
Sofie Pollin, Andre Bourdoux, Liesbet Van Der Perre

IMEC, Kapeldreef-75, Leuven, B-3001, Belgium

ABSTRACT

Harmonic rejection mixing is indispensable in software defined radio receivers employing switched mixers. Current analog multi-path mixing solution suffers from phase and gain mismatches along the paths and as a consequence cannot provide sufficient harmonic rejection. In this paper, we present a low complexity flexible digital intensive harmonic rejection architecture and show how it can be used to enhance the rejection of any single harmonic interference by adaptively combining the different mixing paths. Simulation results show that the proposed method can reject any single interferer adaptively by over 80 dB, which is sufficient for practical applications.

Index Terms— Harmonic Rejection, Digital Intensive, Adaptive Filter, Software Defined Radio.

1. INTRODUCTION

Switching mixing is widely employed in practical receivers' design, because, compared to sinusoidal, square waves are easier to produce over a wide frequency range [1]. However, when considering Software Defined Radios (SDRs) which require a wideband receiver, switching mixing causes a harmonic down-mixing problem: RF interfering signals present at multiples of the desired signal's frequency will also be down-mixed to the baseband due to many local oscillator (LO) harmonics in the switching LO wave, distorting the desired signal [2]. This kind of interfering signals are named as harmonic interferers (HIs) in the rest of this paper.

Multi-path harmonic rejection (HR) [3]-[8] is a promising solution to handle harmonic down-mixing without the need of bulky and power hungry RF filters proposed in [9] and [10]. The principle of this solution is to combine the outputs of multiple switching mixers, each weighted with an appropriate weighting factor to approximate the aggregate LO as a pseudo-sinusoid signal (Fig.1). As shown in Fig.1, in case of a 8-phase mixer, LO_2 and LO_3 are typically 45^o and 90^o shifted duplicates of LO_1, each of them containing many odd-order harmonics. It has been shown that an aggregate LO using exactly $|LO_2| = \sqrt{2} \times |LO_1| = \sqrt{2} \times |LO_3|$, rejects the 3rd- and 5th-order HIs completely [2].

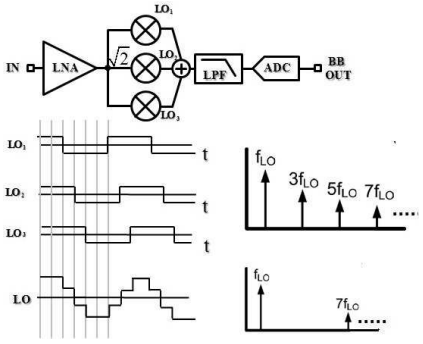

Fig. 1. Eight-phase harmonic rejection principle

The HR performance of this multi-path solution depends on the phase and gain accuracy of each path. State-of-art achievable HR performance is typically limited to 30-40 dB due to unavoidable phase and gain mismatches along paths in any practical implementation [6], which is far away from the required 60 dB to reject HIs down to the receiver noise floor.

Numerous multi-path HR and mismatch compensation options have been explored, which can be categorized into three main categories:

1. **Analog Recombination + Analog Compensation (ARAC)** [3]-[5]: Mismatch mitigation and multi-path signal recombination are both performed in the analog domain. This approach suffers from limited resolution and accuracy of applied analog circuits, implementation difficulties, area and power inefficiency.

2. **Analog Recombination + Mixed-signal Compensation (ARMC)** [6]-[8]: Digital post-compensation is utilized to enhance HR performance achieved already by ARAC.

3. **Digital Recombination + Digital Compensation (DRDC)** [2]: Our previous work proposed a digital recombination HR architecture, supported by a generic mathematical framework for this effort. Under this scheme, the receiver architecture is greatly simplified by exporting each path's down-mixed signal directly without any fine gain or phase tuning in the analog domain, as required in ARAC and ARMC.

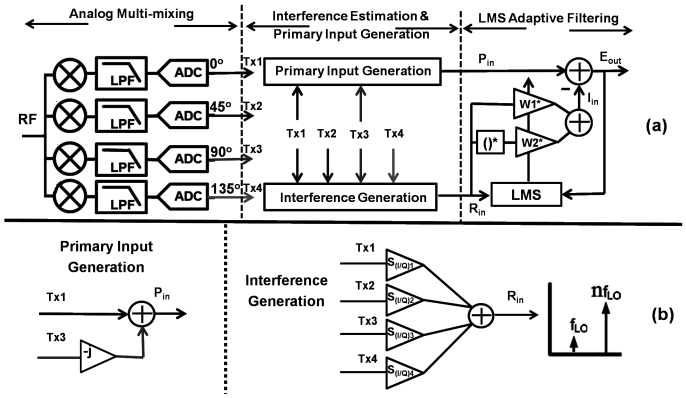

Fig. 2. System framework for the proposed HR scheme

In this paper, we propose a low complexity DRDC method with four mixing paths capable of fully rejecting any single HI, which is achieved through an adaptively optimizing HI rejection scheme. The experimental result for rejecting the 3rd-order HI shows that over 80 dB HR can be achieved for large initial phase and gain mismatches, which is sufficient for practical RF scenario. This avoids the need for any analog phase or gain tuning and hence significantly simplifies the complex analog circuits' design compared to ARAC and ARMC. As an extension work of [2], an adaptive HR scheme robust to large gain and phase mismatches is explored. In addition, compared with state-of-the-art [6]-[8], which are only capable of rejecting the 3rd- or 5th-order HI, a HR scheme aiming for any single HI is proposed.

The remainder of this paper is organized as follows: Section 2 presents the detailed HR architecture and the digitally adaptive HR method capable of rejecting any single HI; Section 3 demonstrates the experimental results for the 3rd-order HI' rejection and compares them with relevant state-of-the-art; and Section 4 concludes the paper.

Notation: $\Re()$ denotes the real part of a complex number and $\Im()$ denotes the imaginary part of a complex number. Superscript * represents the complex conjugate.

2. PROPOSED DRDC SCHEME WITH ADAPTIVE HI REJECTION

This section firstly presents the DRDC system framework, and then explains the interference estimation method for any single HI, which determines the achievable system HR ratio.

2.1. DRDC System Framework for HR

Fig.2 illustrates the DRDC system framework for the proposed HR scheme. Each mixer in the analog front-end is a differential element. After low pass filtering, the down-converted baseband signal in each path is directly converted to digital by an A/D converter, instead of being recombined in the analog domain first. Equidistant 45^o shifted LOs ($0 - 45 - 90 - 135^o$) are provided to the four paths, taking into account unavoidable phase error and gain mismatch for each LO. Each mixing path provides a baseband input signal containing rich distortions due to harmonic down-mixing.

In the digital domain, the primary input, containing the desired signal and multiple distortions, is constructed by a linear recombination of the input paths. To eliminate the harmonic distortions in this primary signal, adaptive interference rejection is performed. To this end, a reference input containing the interference estimation is generated by a second linear recombination of the input signals, as shown in Fig.2(b). A generic coefficient estimation method for estimating any single HI will be presented in detail in Section 2.2. The working mechanism of the adopted least mean squares (LMS) adaptive filtering method is to adaptively adjust the amplitude and phase of the interference estimation to produce an output that is as close a replica as possible to the distortion components in the primary input. This output is then subtracted from the primary input to produce the desired signal [11].

Two single-tap filtering with each multiplied by a complex equalization factor $(w1, w2)$ are conducted in the adaptive filtering engine (AFE), as shown in Eqn.(1). We introduce time index k in the following equations for better illustration.

$$I_{in}[k] \quad = \quad (R_{in}[k] \times w1^*[k] + R^*_{in}[k] \times w2^*[k]) \qquad (1)$$

where R_{in} is the interference estimation and I_{in} is the filtering output, which is a phase and gain adjusted R_{in} to approximate the distortion in the primary input.

Adaptive adjustment of $w1, w2$ is performed through the well-known LMS scheme [12], shown in Eqn.(2), but any other adaptive filtering algorithm (minimizing on Minimum Mean Square Error criterion) can be used.

$$\begin{aligned} w1[k+1] &= w1[k] + \mu \times E^*_{out}[k] \times R_{in}[k] \\ w2[k+1] &= w2[k] + \mu \times E^*_{out}[k] \times R^*_{in}[k] \\ E_{out}[k] &= P_{in}[k] - I_{in}[k] \end{aligned} \qquad (2)$$

where $E_{out}[k]$ is the error signal generated at time k and is also the system output. μ is the LMS step-size parameter.

Due to the phase and gain mismatches in the analog front-end, the interference estimation signal R_{in} will however still contain a small residual of the desired signal component. This signal component will cause some cancellation of the desired signal in the primary input. Assuming the signal to interference ratio (SIR) at the interference estimation input, the primary input and the output E_{out} are defined as SIR_{est}, SIR_{pri} and SIR_{out}, it is proven in [11] that the maximum achievable SIR_{out} is determined by SIR_{est} as follows:

$$SIR_{out} \quad = \quad \frac{1}{SIR_{est}} \qquad (3)$$

Two important conclusions can be drawn from Eqn.(3): 1.) The value of SIR_{pri} does not have influence on SIR_{out}. Thanks to this, the primary input in the proposed framework can simply be constructed by combining the outputs of the

conventional in-phase (I) path (TX1) and the quadrature-phase (Q) path (TX3) without any HR efforts. Compared to the framework proposed in [6], the system architecture enabled here is hence greatly simplified; 2.) To maximize system HR performance, namely to maximize SIR_{out}, SIR_{est} should be minimized. This indicates that the interference estimation recombination signal should contain as little desired signal component as possible. Therefore, an optimized interference estimation method is strongly needed and will be presented in the next section .

2.2. Interference Estimation Method

This section explores the optimal interference estimation with a generic coefficient estimation method.

Building on the developed mathematical framework presented in [2], the coefficients for path recombination for interference estimation can be derived by Eqn.(4)

$$\begin{bmatrix} Cancelling\ desired\ signal\ in\ I\ path \\ Extracting\ imag\ component\ of\ m_{th}\ HI \\ Cancelling\ desired\ signal\ in\ Q\ path \\ Extracting\ real\ component\ of\ m_{th}\ HI \end{bmatrix} \tag{4}$$

, which leads to:

$$\begin{bmatrix} \sum_{n=1}^{N} S_{In} F_{LOn1} \\ \Re(\sum_{n=1}^{N} S_{In} F_{LOnm}) \\ \sum_{n=1}^{N} S_{Qn} F_{LOn1} \\ \Im(\sum_{n=1}^{N} S_{Qn} F_{LOnm}) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{matrix} \forall m \quad concerned \\ \\ \forall m \quad concerned \end{matrix} \tag{5}$$

where S_{In} and S_{Qn} are weighting factors that need to be generated for I and Q paths, N is the total number of paths, m represents the m_{th}-order HI that needs to be estimated and F_{LOnm} denotes the complex Fourier coefficient of LO's m_{th} harmonic in the n_{th} mixing path, which can be derived to be Eqn.(6):

$$F_{LOnm} = P_m \times e^{-jm\theta_n} \times (1 - (-1)^m) \tag{6}$$

where $P_m = (-1)^{\frac{m-1}{2}} \times \frac{2}{m \times \pi}$ and θ_n denotes the phase shift of LO in the n_{th} mixing path.

For any single m_{th}-order HI component's extraction, the equations are determined and a set of scaling factors ($S_{I(1-4)}$ and $S_{Q(1-4)}$) can always be found to make Eqn.(5) meet. This means that, ideally, the interference estimation signal will contain only the interference component and perfect cancellation is possible.

3. EXPERIMENTAL RESULTS AND COMPARISON

This section firstly presents the experimental results for rejecting the 3rd-order HI based on the proposed DRDC HR method, and secondly analytically compares the proposed method with the latest ARMC method in [6][7], which represents the best HR performance up to date to the authors' knowledge.

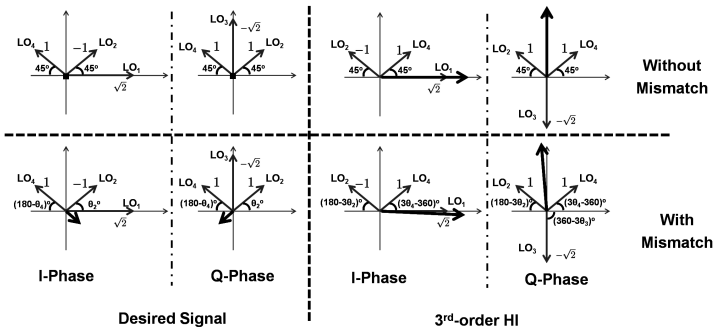

Fig. 3. Vector diagrams for the 3rd-order HI generation

To show the robustness of the proposed method, an unfavorable situation for performance with relative large phase error (2^o) and gain mismatch (6%) in the analog front-end is assumed in the simulation model. A random 256-QAM modulated desired signal and a 3rd-order HI with input power varying from 15 to 65 dB stronger is used as the RF input.

For the 3rd-order HI estimation, Eqn.(5) should be quantified to Eqn.(7) for the case being explored: four paths for estimating the 3rd-order HI.

$$\begin{bmatrix} \sum_{n=1}^{4} S_{In} F_{LOn1} \\ \Re(\sum_{n=1}^{4} S_{In} F_{LOn3}) \\ \sum_{n=1}^{4} S_{Qn} F_{LOn1} \\ \Im(\sum_{n=1}^{4} S_{Qn} F_{LOn3}) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7}$$

where F_{LOn1} and F_{LOn3} can be derived from Eqn.(6), and θ_n in this case is around $(45 \cdot n)^o$, superimposing the modeled phase error. A set of scaling factors $S_{I1} = \sqrt{2}$, $S_{I2} = -1$, $S_{I3} = 0$, $S_{I4} = 1$, $S_{Q1} = 0$, $S_{Q2} = 1$, $S_{Q3} = -\sqrt{2}$ and $S_{Q4} = 1$ establishes Eqn.(7) without considering phase error, and is used in the generation of interference estimation signal.

Fig.3 illustrates the interference estimation via vector diagrams. For ideal phase shifts of LOs, as shown in the upper graph, the 3rd-order HI can be estimated perfectly without any residual of desired signal component with above generated scaling factors. Taking into account the practical phase-shift errors, the generated interference estimate will contain a small residual of desired signal component, as shown in the graph underneath. The larger is the phase error, the more significant the presence of the residual.

Fig.4 shows the simulation performance of our proposed adaptive HR scheme for the 3rd-order HI's rejection in the form of scatter plot of improved SIR after adaptive compensation and probability of achieved HR. The simulation was conducted with different input power of the 3rd-order HI to cover the real RF scenario and without considering other analog imperfections than the phase and gain imbalances. It can be seen that more than 80 dB HR can be achieved for the RF scenario concerned, which is enough to provide a SIR of more than 20 dB in the digital domain to guarantee correct demodulation. Note that the HR performance for rejecting any other

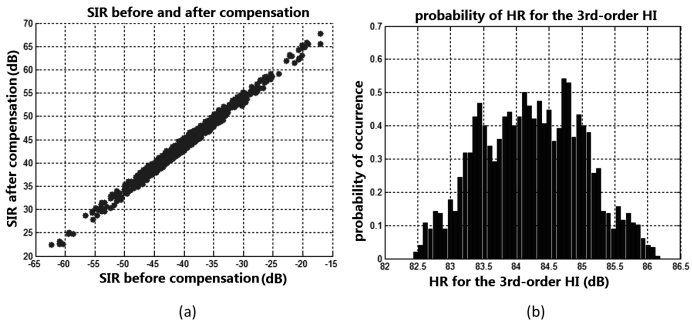

Fig. 4. Simulation result of the 3rd-order HI rejection. (a): Scatter plot of SIR before and after compensation. (b): Probability of achieved HR

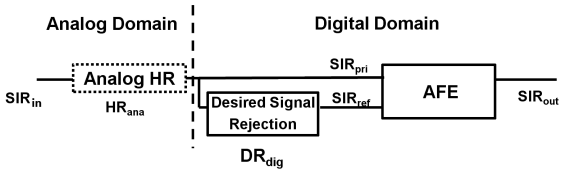

Fig. 5. Sketch for ARMC HR system framework

single HI is comparable, since Eqn.(5) can always meet for any single HI's rejection.

Compared to the state-of-the-art ARMC methods of [6]-[8], the proposed DRDC scheme saves complex analog circuits' design effort that would be required for scaling the gain of each mixing path using a resistor network, and theoretically improves the system performance bound, which will be illustrated in detail below:

Fig.5 depicts the sketch of the state-of-the-art ARMC HR system framework. Assuming the SIR at the receiver input is denoted as SIR_{in}, the HR ratio of analog front-end is denoted as HR_{ana} and the rejection ratio of the desired signal in the interference estimation is denoted as DR_{dig}, the following relationship among the above values exists:

$$SIR_{in} + HR_{ana} - DR_{dig} = SIR_{est} \tag{8}$$

As shown in Eqn.(3), the maximum achievable SIR_{out} is the reciprocal of SIR_{est}. Therefore, the achievable system HR ratio ($SIR_{out} - SIR_{in}$) of ARMC scheme can be represented by Eqn.(9):

$$\begin{aligned} HR &= SIR_{out} - SIR_{in} \\ &= -2 \times SIR_{in} + DR_{dig} - HR_{ana} \end{aligned} \tag{9}$$

As can be seen from the performance bound equation Eqn.(9), analog HR efforts reduce the overall achievable system HR ratio actually. Namely, the achievable HR ratio of proposed DRDC scheme is HR_{ana} dB more than that of the ARMC methods in [6]-[8].

4. CONCLUSIONS

This paper proposes a low complexity HR method with digital multi-path recombination and adaptive digital HI estimation for SDR receiver design, which greatly reduces sensitivity to analog circuit impairments. Theoretical derivation shows improved achievable HR performance compared to state-of-the-art ARMC recombination schemes. Simulation results show achievable rejection up to 80 dB guaranteeing sufficient SIR in digital domain. The proposed digitally adaptive HR scheme will facilitate low-cost, high-HR SDR receivers.

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