A NOVEL AND EFFICIENT MULTI-RESOLUTION CHANNELIZER FOR SOFTWARE DEFINED RADIO

fred harris[a], *Elettra Venosa*[a], *Xiaofei Chen*[a], *Chris Dick*[b], *Brent Adams*[c]
[a]San Diego State University, [b]Xilinx Corp., [c]Raytheon Corp.

ABSTRACT

There are number of software defined radio applications in which a radio receiver must access multiple simultaneous channels with different channel bandwidths. This paper presents the architecture of a novel and extremely efficient implementation of such a channelizer. The receiver described here simultaneously forms ten 5-MHz wide channels and one hundred 0.5 MHz wide channels spanning a 50 MHz input bandwidth. Multirate signal processing techniques are used throughout the processing chain to obtain extremely low processing computational workload.

Index Terms— *Multi-Resolution Channelizer; software defined radio; polyphase channelizer; multirate signal processing.*

1. INTRODUCTION

Channelizers play an important role in many communication systems. These systems include cable networks, wireless cell sites, and satellite transponders. Many channelized systems are characterized by multiple equally spaced, equal bandwidth, channels that span an allocated band of frequencies. The standard AM and FM broadcast bands are an example of this signal set. Radios have become more capable and flexible and they can operate in new modes enabled by their ability to rapidly reconfigure under software control. In one desirable mode the radio and its network can support a bandwidth on demand option. Next generation wireless networks such as WiMax and LTE were designed to offer this option.

In this paper we first present a reasonable set of channelizer specifications. We then show an initial, perhaps neophyte's brute force, signal processing approach to the signal conditioning and channelization tasks that satisfy the stated specifications. We then develop and illustrate the performance of a novel architecture that accomplishes the same tasks with significant reduction in required computational resources.

We now define the signal characteristics and specifications of interest to us. The channels of interest span a 50 MHz bandwidth centered at 750 MHz and accessed at the output of an analog intermediate frequency (IF) filter. Our system must perform the following tasks: (i) sample the real IF signal, (ii) translate the 50 MHz band to base band (iii) filter the complex baseband signal to the 50 MHz bandwidth, (iv) reduce the sample rate commensurate with the bandwidth reduction, (v) channelize the 50 MHz wide, reduced sample rate, baseband signal to multiple 5 MHz channels down sampled to 10 MHz sample rate, and finally (vi) channelize the same 50 MHz wide, reduced bandwidth signal to multiple 0.5 MHz channels sampled at 1.0 MHz sample rate.

Figure 1 presents the block diagram of an architecture that performs the tasks we just enumerated. In this architecture the IF signal is down converted to base band by two mixers driven by a 750 MHz quadrature oscillator. The base band I-Q pair is filtered by a pair of anti-alias analog filters with two sided bandwidth of 50 MHz. The signal pair is sampled at a 100 MHz rate by a pair of analog to digital converters (ADCs). The gain and phase imbalance of the sampled data signal are removed by I-Q balancing algorithms. Finally the sampled data sequence is processed by two channelizers: one is a 20 channel channelizer that outputs 5 MHz wide channels at 10 MHz sample rate and the other is a 200 channel channelizer that outputs 0.5 MHz wide channels at 1.0 MHz sample rate.

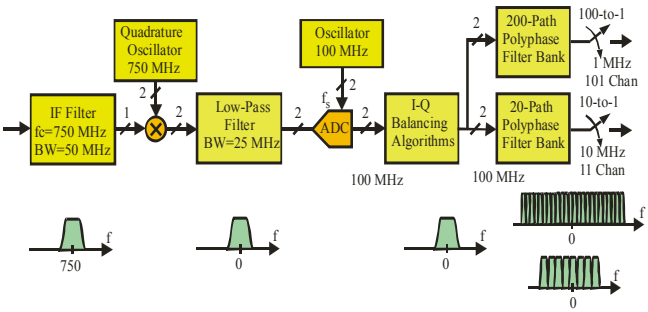

Figure 1. Block Diagram of Dual Resolution Channelizer: Input Signal Conditioning Performed by Analog Quadrature Down Converter and I-Q ADCs.

Gain and Phase mismatches in the analog anti-aliasing filters as well as the DC injected by the self mixing in the analog mixers and by the bias of the ADCs significantly degrade the quality of the signals processed by the architecture of Figure 1. An alternate architecture avoids signal degradation related to the gain and phase mismatches of the two analog paths by translating the signal from the first IF filter centered at 750 MHz to an offset IF filter centered at 150 MHz. A block diagram of this architecture is presented in Figure 2. The output of the second IF is sampled at 600 MHz by a single ADC. The sampled data representation of the IF signal, with spectrum residing at the quarter sample rate, is then digitally down converted to baseband by a trivial DDS operator. The down converted

samples are filtered by linear phase re-sampling filters that reduce the noise bandwidth to a 50 MHz two sided BW which enables the reduction of the input sample rate by a factor of 6-to-1 to obtain the 100 MHz rate for which the dual channelizers of Figure 1 had been designed.

2. PROPOSED ARCHITECTURE

The main difference between the two architectures of Figures 1 and 2 is that we replace two baseband filters with a single offset IF filter, replace the quadrature oscillator with a single port oscillator, and replace the two ADCs operating at 100 MHz with a single ADC operating at 600 MHz. We can accomplish the same signal conditioning tasks performed in Figure 2 with fewer analog components by directly sub-sampling the output of the first IF Filter.

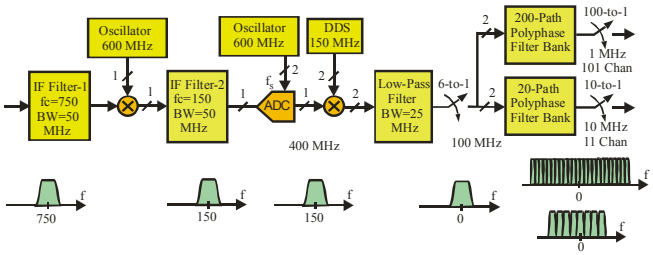

Figure 2. Block Diagram of Dual Resolution Channelizer: Signal Conditioning Performed by Single Mixer, Offset IF filter, ADC, Digital Down Converter and Resampled Digital Low Pass Filters.

This option uses aliasing to achieve the same operation performed by the mixing operation that moved the signal spectrum to the offset IF filter. Realizing the advantage of the aliasing operation in the initial sampling operation we are motivated to embed aliasing in the low pass filters in the channelizer structure. We will do this first and then continue to the dual channelizers themselves where we will again find opportunities to reduce computational requirements by embedding alias inducing resampling in the channelization process. Figure 3 shows the block diagram of the dual resolution channelizer using IF sampling. The sample rate of the ADC is 600 MHz, the same as it was in the architecture of Figure 2. Here the 750 MHz center frequency of the IF frequency input signal is 150 MHz above the 600 MHz sample rate. Since in the sampled data domain multiples of the sample rate are congruent to DC, the signal positioned 150 MHz above the sampling clock at the input to the sampler is seen to be aliased to 150 MHz above DC which is the quarter sample rate of the 600 MHz sample clock. This aliasing operation can be visualized in Figure 4 which shows the frequency axis of a 600 MHz sampling clock. We see the band centered at 750 MHz, in Nyquist zone 1 above the sampling clock frequency, folds onto the band centered at 150 MHz in Nyquist zone 0. The sub-sampling of the IF centered signal is seen to replace the spectral translation that was performed by the mixer and second IF filter in Figure 2.

The next aliasing operation occurs in the 4-path filter following the ADC. A block diagram of this filter is shown in Figure 5. The traditional 4-path filter performs a 4-to-1 down sample operation by delivering 4-successive input samples to the 4 commutator ports in the order {3, 2, 1, 0}. In this mode the 4 spectra located at multiples of the quarter sample rate alias to baseband (DC). A phase coherent sum of the 4-path filters extracts one of these aliases and destructively cancels the others.

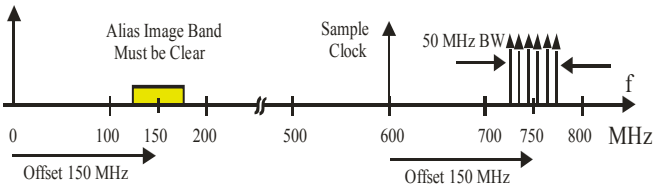

Figure 4. Spectrum of Band Centered at 750 MHz Aliases to 150 MHz When Sampled at 600 MHz.

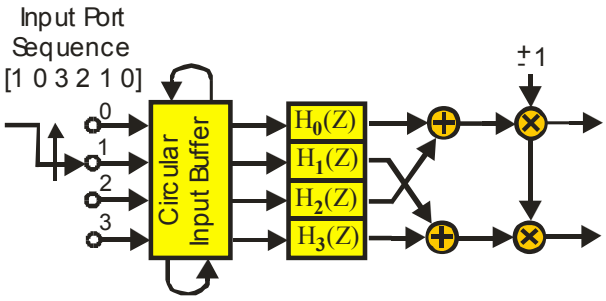

Figure 5. Block Diagram: 6-to-1 Down Sample 4-Path Filter.

The rotators that extract the quarter sample rate signal are the sequence {1, j, -1, –j}. We modify the 4-path filter to perform a 6-to-1 down sample rather than the traditional 4-to-1. In this mode the quarter sample rate aliases to the half sample rate and sign reversals of alternate output samples translates the alias from the half sample rate to DC. These sign reversals are performed by the ±1 multipliers shown in Figure 5. The circular input buffer at the input block of Figure 5 performs the serpentine shift of the input data stream through the columns of the polyphase filter. The serpentine shift in the two dimensional filter is equivalent to the 6-sample shift in the prototype one dimensional filter prior to its polyphase partition. Figure 6 shows the input sample indices in the polyphase filter partition in three successive addressing states. The left most segment shows the indices after the last 6-samples have been delivered by the input commutator. The central segment shows the circular shift of row contents prior to the delivery of the next 6-samples. The right most segment shows the indices after the next 6-samples have been delivered by the input commutator.

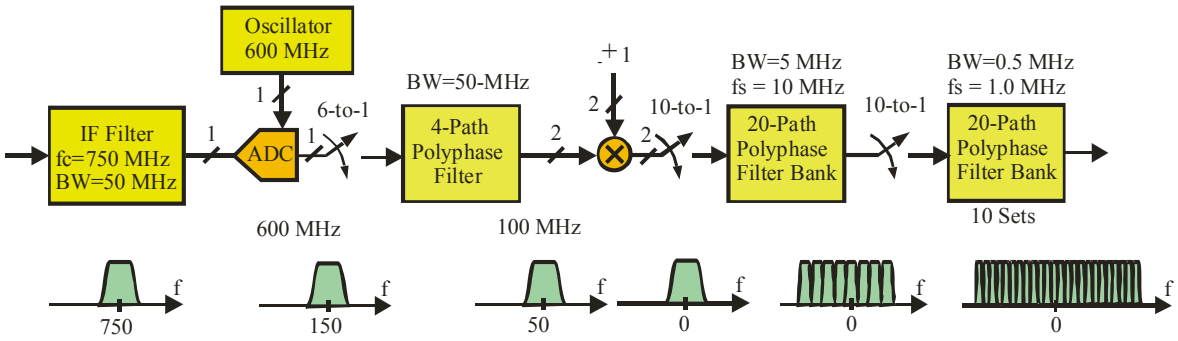

Figure 3. Block Diagram of the IF-Sampled Dual Resolution Channelizer. The Spectral Band Centered at 750 MHz Aliases to 150 MHz When Sampled by the 600 MHz Sampling Clock. Down Sampling the Input 600 MHz 6-to-1 to the Output 100 MHz in the 4-Path Low Pass Filter, Aliases the Band Centered at 150 MHz, the Input Quarter sample rate to 50 MHz, the Output Half Sample Rate. Trivial Sign Changes Translates the Band at the Half Sample Rate to DC.

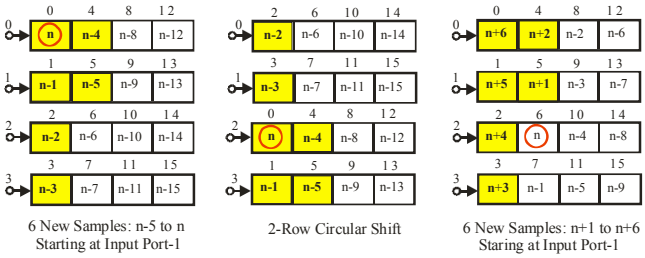

Figure 6. Input Sample Indices for Three Successive States of Input Data Buffer: State 0, 6-New Input samples, State-1, Two Row Circular Shift of Input Buffer, State-2, 6-New Input Samples.

Figure 7 shows the input sample indices for three successive 6-input sample shifts in the one dimensional filter and the corresponding serpentine shifts in the two dimensional filter. Here the integers above the registers are the indices of the filter coefficients and the integers in the register are input sample indices. The last 6-input indices are highlighted as bold integers in both forms of the filter. We also note that on successive shifts, sample "n" resides alternately in path "0" and in path "2". The phase shifters for these paths are alternately ±1 which explains the sign reversals of the signal samples of the spectral term that has aliased to the half sample rate.

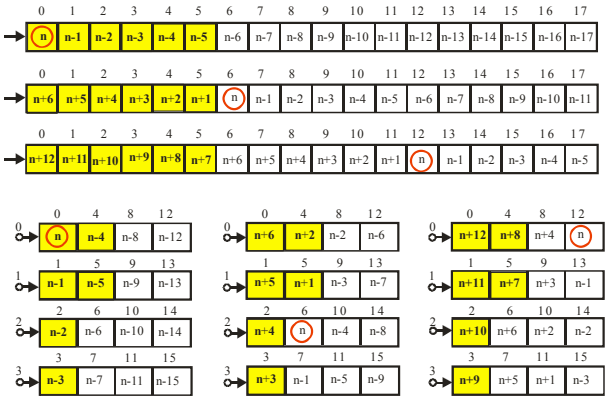

Figure 7. Input Sample Indices for Three Successive Shifts of 6-Input Samples to Implement 6-to-1 Down Sample in the 1-Path Prototype and the 4-Path Partitioned Filter.

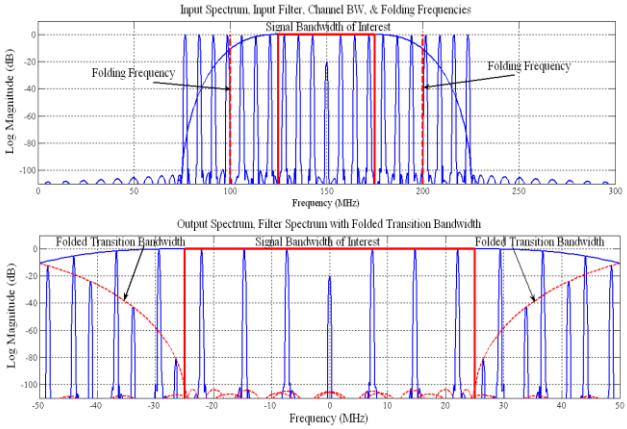

Figure 8. Input and Output Spectra of 6-to-1 Down Sample 4-Path Filter Showing Folding Frequency, Filter Shape and Folded Band Edge.

Figure 8 shows the spectra at the input and output of the 4-path polyphase filter. Also shown are overlays of the filter's frequency response, the folding frequencies of the 6-to-1 down sample, and the filter's folded band edges. We also indicate the spectral span containing the signal spectrum of interest. We have used a spectral comb of sine waves for the processed signal to better illustrate the spectral folding due to the 6-to-1 resampling. These terms are clearly seen under the filter's folded band edges.

3. DUAL RESOLUTION CHANNELIZER

We first review the requirements for the dual resolution channelizer. One channelizer is to form 5 MHz wide channels on 5 MHz spectral centers and the other is to form 0.5 MHz wide channels of 0.5 MHz spectral centers. The sample rate for the 5 MHz channelizer is 10.0 MHz and the sample rate for the 0.5 MHz channelizer is 1.0 MHz. The prototype low pass filter embedded in the channelizer will have a 0.1 dB pass band width of 5.0 (or 0.5) MHz with a 100 dB stop band width 10.0 (or 1.0) MHz. With the sample rate twice the analysis bandwidth and the filter transition

bandwidth fully contained in this same sample rate span the analysis bandwidth of the channels will be alias free. Note that the ratio of output sample rate to analysis bandwidth for the channelizers is the same as the ratio of output sample rate to analysis bandwidth for the 4-path polyphase filter. The difference here is that the transition band edges of the channelizer filters do not fold while the transition band edges of the signal conditioning 4-path filter did fold during the resampling process. The spectral span of interest to us is 50 MHz and the sample rate presented to the channelizers is 100 MHz. The sample rate controls the number of channels, thus the 5 MHz channelizer must form 20 channels and the 0.5 MHz channelizer must form 200 channels. Of the 20 and 200 channels formed by the channelizers we only use the 11 channels and 101 channels that span the 50 MHz frequency alias free span.

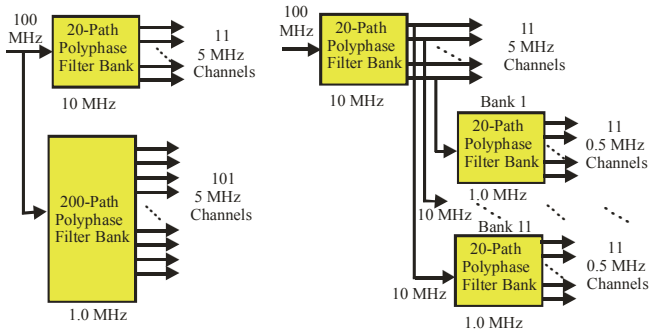

Figure 9. Block Diagrams of Initial and Alternate Dual Resolution Channelizers

The first intuitive approach to the design of the dual resolution channelizer is to design a channelizer for each resolution and to operate them as parallel processing blocks. This in fact is suggested in Figures 1 and 2 which at the end of the signal conditioning segment contain two channelizers. It is easy to reason that the 200 path channelizer will require between 10 and 20 times the computational resources of the 20 path channelizer. The 200 path polyphase filter requires 10 times the resources of the 20 path filter and the 200 point IFFT in the channelizer requires approximately 60 times the resources of the 20 point IFFT. The extra factor of 6, derived shortly, comes from the complex phase rotators of the CT algorithm used to phase align the FFTs of its non relative prime factors (10 and 20).

If we consider the cost of the 20 path channelizer to be unity, then the cost of the 200 path channelizer would be bounded by 20. We can reduce the cost of the 200 path channelizer by an alternate design. We can obtain the 0.5 MHz channels by processing the 5.0 MHz wide output channels of the first 20 path channelizer with another 20 path channelizer. This option is illustrated in Figure 9. A second tier channelizer processes each of the 11 output ports of the first channelizer for a total of eleven second tier channelizers. The first tier channelizer operates on a 100 MHz input series while the second tier channelizers on 10 MHz output series. Thus the workload for ten of the second tier channelizers is the same as the workload of the first tier channelizer. We conclude that the cost of the twelve series channelizers required to provide the dual resolution channels is 2.1 as opposed to 21 for the parallel channelizer option. This factor of 10 is a cost reduction that cannot be ignored. The 20 point IFFT used in the alternate architecture can be implemented by the prime factor Good Thomas (GT) algorithm with the two factors (4 and 5) in turn implemented by the Winograd transform. This is an extremely efficient IFFT requiring only 40 real multiplies to process 20 complex input samples. By way of comparison, the 200 point IFFT can be implemented by a 20 by 10 CT algorithm which is nowhere as efficient as the GT.

Using the efficient 10 and 20 point GT IFFTs and the complex phase rotators of the CT the 200 point IFFT requires approximately 2400 real multiplies. This IFFT would operate at the 1.0 MHz transform rate of the 200 channel channelizer. Again by comparison, the GT transforms operating in the eleven second tier channelizers perform 40 real multiplies at the same 1.0 MHz transform rate. The 20 point GT IFFTs in the eleven second tier channelizers require a total of 800 real multiplies. Thus we see that the workload for the eleven short IFFTs is approximately one third of the workload for the single large IFFT that it is replacing.

4. CONCLUSIONS

We have presented a channelizer problem that required the simultaneous spectral partition of a specified frequency span into resolutions. The example we addressed was 10 channels of 5 MHz bandwidth and 100 channels of 0.5 MHz bandwidth. We showed two possible architectures in which much of the signal conditioning was performed in the analog domain using traditional radio receiver perspectives. Similarly, the dual resolution channelizers were visualized as two independent and parallel processing tasks. We then introduced an alternate architecture in which the signal conditioning relied on properties of multirate systems. We used IF sub sampling to effect the first alias translation from the analog IF filter to the quarter sample rate of the sampling clock. We then used a 4-path polyphase filter which traditionally aliases the quarter sample rate to baseband with a simultaneous 4-to-1 down sample. Responding to the philosophy that sample rate reductions in one stage reduce the workload in the next stage, we modified the 4-path filter to permit a 6-to-1 rather than the 4-to-1down sampling. We then addressed the two channelizes and recognized that the higher resolution channelizer could take advantage of the bandwidth and sample rate reduction made available by the low resolution channelizer. We estimated the workload reduction offered by operating series channelizers rather than parallel channelizers.

5. REFERENCES

[1] f. harris, "Multirate Signal Processing for Communication Systems", Prentice-Hall, 2004.

[2] f. harris, "Fixed Length FIR Filters with Continuously Variable Bandwidth', Wireless Vitae'09, Aalborg Denmark, 17-20 May, 2009.

[3] Gordana Jovanovic-Dolecek, "Multirate Systems: Design and Applications", Idea Group Inc., 2002.

[4] S Mitra, Y. Neuvo and H. Roivainan, "Design of Recursive Digital Filters with Variable Characteristics", Proc. ISCAS'98, Vol. 5 pp. V379-V382, Monterey, California, May 1998.

[5] fred harris, Chris Dick, Xiaofei Chen, Elettra Venosa "Wideband 160 Channel Polyphase Filter Bank Cable TV Channelizer", IET Signal Processing, Vol 5, Issue 3, pp. 325-332, June 2011.

[6] Sidney Burrus and Thomas Parks, "DFT/FFT and Convolution Algorithms and Implementations", Wiley-Interscience, 1985.

[7] R. Mahesh, A. P. Vinod, E.M-K. Lai, and A. Omondi, "Filter Bank Channelizers for Multi-Standard Software Defined Radio Receivers," *JOURNAL OF SIGNAL PROCESSING SYSTEMS*, Vol. 62, n.2, pp. 157-171, 2011.

[8] Abu-Al-Saud, W.A.; Stuber, G.L.; , "Efficient wideband channelizer for software radio systems using modulated PR filterbanks," *Signal Processing, IEEE Transactions on*, vol. 52, no.10, pp. 2807- 2820, Oct. 2004.

[9] E. Venosa, f. harris and F. Palmieri, *Software Radio: Sampling Rate Selection, Design and Synchronization*, Springer Science + Business Media, 2011.