TOWARDS AN INTEGRATED CIRCUIT DESIGN OF A COMPRESSSED SAMPLING WIRELESS RECEIVER

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ABSTRACT

In this paper, we investigate the extension of previous work on compressed sampling receivers from mathematical abstractions and proof of concept work into a system that directly competes with more traditional receivers in standard CMOS integrated circuit technology. As developed in the literature, the Modulated Wideband Converter shows great promise as a compressed sampling receiver due to its flexibility and inherent spectral agility. We propose several modifications to the system that improve its usability and performance in real-world scenarios. Then, using standard LTE receivers as a basis for comparison, we propose a set of target specifications for the Modulated Wideband Converter, discuss the associated circuit challenges, and evaluate potential solutions that build upon prior work in integrated circuit and system design.

***Index Terms*—** Compressed Sampling, Software-Defined Radio, Cognitive Radio, Modulated Wideband Converter, LTE

1. INTRODUCTION

Software-defined radio (SDR) has been actively pursued for almost twenty years. Even though most of the conceived architectures tend to suffer from a penalty in complexity and performance, the SDR approach remains an attractive target due to the flexibility it promises. In a standard direct conversion receiver, like that of Fig. 1a, the frequency range of standard voltage-controlled oscillators (VCOs) and mixers limits the receiver to a small slice of the frequency spectrum. Ongoing research seeks to expand the frequency handling capabilities of standard receivers [1]. Even with a wide-band front-end, the stringent blocker requirements of today's wireless standards make variable-width filters an unattractive option. Conversely, fixed-width filters make it impossible to dynamically adjust the desired bandwidth in the signal chain. Thus, dynamic bandwidth allocation is often achieved through carrier aggregation, where identical receivers independently tune to adjacent channels, thus allowing the system to dynamically change its total bandwidth.

Compressed sampling promises to further increase the flexibility of an SDR by enabling the receiver to determine the spectral support of a multi-carrier signal in a sparse environment without prior knowledge of the individual carrier signals. Once the spectral support is determined, the desired signal can be extracted. Blind recovery capability increases the overall flexibility of an SDR dramatically, making SDR an even more attractive goal. Our work focuses on the Modulated Wideband Converter (MWC), which has been to shown to be a hardware efficient realization of a compressed-sampling receiver [2,3].

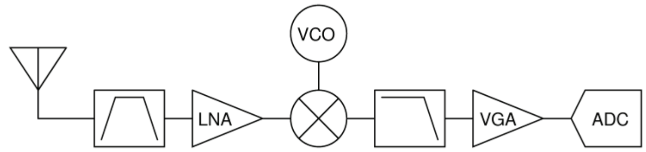

Fig. 1a: A standard direct conversion receiver topology.

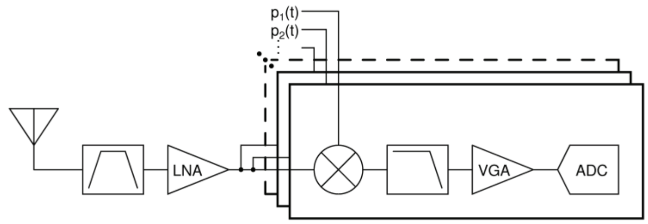

Fig. 1b: The MWC topology.

In this paper, we propose a system-level modification of the MWC to improve its ability to perform in a real-world environment. In addition, we evaluate the noise performance, in-band blocking, and distortion performance of the MWC. In our distortion analysis we extend the work of [3] to account for filtering in the system. Finally, we propose an implementation of the MWC using previously published integrated circuit building blocks, so that its performance can be directly compared to that of an LTE receiver.

2. THE MODULATED WIDEBAND CONVERTER

The MWC architecture, as depicted in Fig. 1b, uses linearly-independent, spectrally-diverse mixing signals $p_i(t)$ to determine the spectral support of the signal from low-rate samples [2]. The spectral diversity guarantees that the entire spectrum is aliased down to baseband, where it can be sampled at a low rate. The topology is particularly attractive because the analog bandwidth requirement of the ADC is low. Furthermore, the mixing sequences can be generated from various taps along a digital shift register, providing additional software-level control of the system [3].

While a spectrally-diverse mixing sequence is necessary for detecting which frequency bands are in use, it is counterproductive when trying to decode the signal. The spectral diversity guarantees that out-of-band interference and noise will be aliased on top of the desired signal at baseband. We therefore propose operating the MWC in two phases. In the first phase, the mixing sequence is chosen for its spectral diversity. Then, in the second phase, the mixing sequence for each branch is optimized to receive one band of the known spectral support. Implementing different mixing sequences optimized for each branch individually requires additional digital logic for each branch, but improves the signal-to-noise plus interference ratio of the system.

3. SYSTEM SPECIFICATION DEVELOPMENT

In order to assess the practical usability of the MWC, we seek to compare it to a standard LTE radio receiver implementation; thus highlighting its strengths and weaknesses. Specifically, we compare the sensitivity, in-band blocking, and distortion performance of an LTE receiver to that of the MWC. While the LTE specification contains numerous frequency bands distributed from 699 to 2620 MHz, we chose to limit our discussion to receive bands between 699 and 915 MHz, i.e. 216 MHz total bandwidth [4]. Limiting the target system to this subset simplifies the filter design and system-level calculations.

3.1. System Sensitivity

Drawing inspiration from LTE, we specify the minimum channel bandwidth of the MWC to be 1.4 MHz. By activating additional branches, our system is able to increase its total bandwidth by 1.4 MHz for each additional branch.

With the system bandwidth set, it is possible to determine the sensitivity of the MWC and compare it to that of an LTE receiver. The sensitivity of a radio receiver is computed as $10\log(kTW) + NF + SNR$ for Boltzmann's constant, k; the absolute temperature, T; bandwidth, W; noise figure, NF; and signal-to-noise ratio, SNR. Unfortunately, in the detection mode the MWC is fundamentally a wideband system. Comparing the noise performance of the MWC in detection mode to an LTE receiver with identical noise figure and SNR, the decrease in signal bandwidth from 216 to 1.4 MHz corresponds to a 21.9 dB sensitivity penalty for the MWC. It should be noted however that the detection mode of the MWC is only trying to recover the spectral support of the signal, which is a relatively small amount of information. This suggests that improved recovery algorithms and time averaging can reduce the required SNR for recovery, mitigating the wide-band noise penalty. In the reception mode the sensitivity limit is the same for both systems.

3.2. In-Band Blocking

Following proof-of-concept work developed in [3], we once again propose a mixing signal comprised of a sign-alternating sequence stored in a digital shift register.

The mixer and local oscillator of the MWC are particularly difficult to design because they need to handle both spectrally-diverse signals with harmonic content spread across the entire band, and spectrally-pure signals with energy focused into a single frequency. It has been shown that various bit-flip sequences can produce an acceptably diverse spectrum [5]. However, the harmonic purity of a bit flip sequence—even one optimized for the receive mode of the MWC—limits the system's in-band blocker rejection. The ability to toggle between a spectrally-diverse and spectrally-pure signal comes at the cost of relatively low in-band spurious-free dynamic range (SFDR) in the reception mode, and makes the in-band blocking requirement one of the toughest specifications for the MWC.

The in-band SFDR of the mixer described above is tied directly to the frequency of the clock that drives the shift register. Consider a bit-flip sequence generated by taking the sign of the ideal mixing sinusoid. The harmonics of this generated sequence

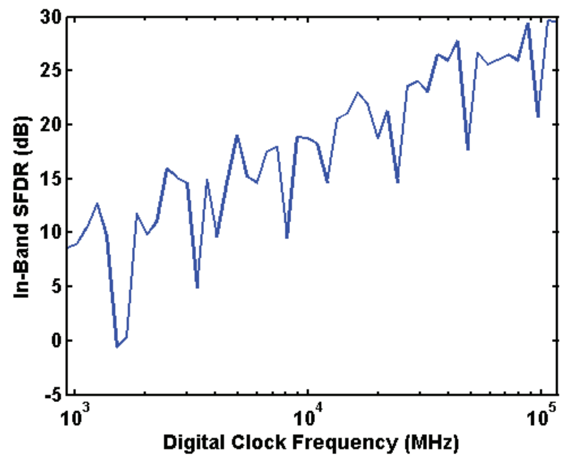

Fig. 2: In-Band SFDR plotted against the digital clock frequency for an 800 MHz carrier.

are at odd multiples of the fundamental. For signals between 699 and 915 MHz these fall entirely out of band and the associated interfering signals can be filtered before the mixer. However, if we generate the bit-flip sequence by sampling the ideal sinusoid at a fixed sampling frequency and populating the shift register with the sign of these samples, then we are forced to lock the transitions of the bit-flip sequence to discrete multiples of the sampling period. Fig. 2 plots the in-band SFDR against the digital clock frequency of the bit-flip sequence. The sequence is generated by sampling an 800 MHz sinusoid and taking the sign of the average value of the sinusoid in that period. From the plot it is clear that increasing the digital clock frequency can drastically improve the performance of the system. Unfortunately, as the digital clock frequency increases so do the associated requirements on the hardware—including power consumption, chip area, and pre-processing complexity. Furthermore, at some point the digital clock is fundamentally limited by the speed of the available devices. Therefore, in order to meet any reasonable in-band blocking requirement, some other technique must be used to increase the in-band SFDR.

We have, up to this point, put forward a square-wave mixing signal as an approximation to an ideal sinusoid. A two-level mixing sequence is convenient because it simplifies the hardware. However, increasing the number of bits used to specify the mixing sequence decreases the quantization error between our mixing signal and the ideal sinusoid. Fig. 3 shows the in-band SFDR swept across the entire frequency band for both two and three-level mixing sequences at a digital clock frequency of 4 GHz. The three-level sequence was generated by computing the contribution of each sequence element to the desired Fourier coefficient and comparing that contribution to a threshold. For contributions above the threshold, the element in question is identical to that of the two-level sequence, whereas a third zero-level is introduced for elements that do not significantly contribute to the desired Fourier coefficient. For each frequency we then swept the threshold and recorded the maximum SFDR. Adding the third-level increases the minimum in-band SFDR by 4.93 dB. Increasing the resolution of the mixing sequence increases the in-band SFDR at the cost of complexity, but is not limited by the maximum operating frequency of the process technology.

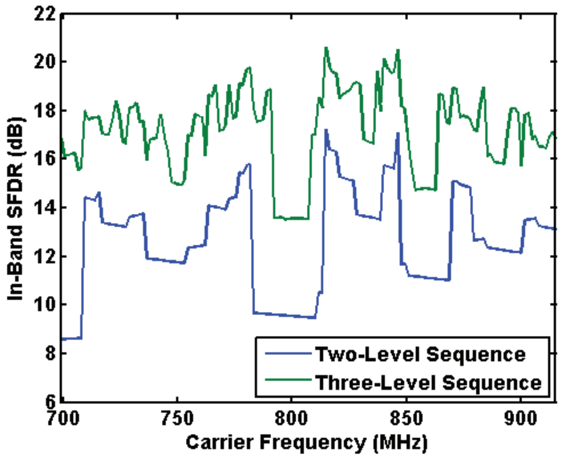

Fig. 3: The difference in in-band SFDR for two and three-level mixing sequences. Both sets of mixing sequences are clocked at 4 GHz.

3.3. Distortion

The MWC is fundamentally a multi-carrier device, and therefore, determining the distortion performance of the entire system is more complicated than for a similar single-carrier system. Consider a single branch of the MWC depicted in Fig. 4. The initial band-pass filter, LNA, and mixer all see a multicarrier signal, while the low-pass filter after the mixer guarantees that the variable gain amplifier (VGA) and the ADC see only the power of a single carrier mixed down to baseband. It is therefore reasonable to treat these two portions separately.

In order to determine the distortion limit of the system we begin by calculating the effective two-tone OIP3 of the multi-carrier subsystem. For the cascaded multi-carrier subsystem, the OIP3 is determined using [6]

$$\frac{1}{OIP3_{subsystem}} = \frac{1}{OIP3_{BPF}} + \frac{1}{OIP3_{LNA}} + \frac{1}{OIP3_{Mixer}} \quad (1)$$

The two-tone intermodulation ratio (IMR) can be computed from the OIP3 with [7]

$$IMR_2 = 2(OIP3 - P_{out}) \quad (2)$$

However, our system is inherently multi-carrier. The worst case multi-tone intermodulation ratio (M-IMR) for *n* equal-power tones is expressed in (3) as the difference between the two-tone IMR and a correction factor (C.F.) as expressed in (4) [7].

$$M - IMR(n) = IMR_2 - C.F. \quad (3)$$

$$C.F. = 10\log\left((n-1)^2 + \frac{n-1}{2} - \frac{1}{2}mod\left(\frac{n+1}{2}\right)\right) \quad (4)$$

Substituting (2) into (3) and rearranging yields

$$M - IMR = 2\left(\left(OIP3 - \frac{C.F.}{2}\right) - P_{out}\right) \quad (5)$$

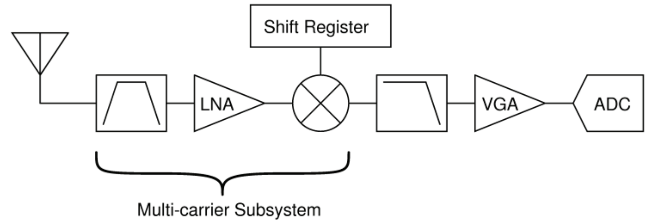

Fig. 4: A single branch of the MWC. The band-pass filter, LNA and mixer see multi-carrier distortion. The low-pass filter, VGA and ADC see only single-carrier distortion.

Thus, we can model the multi-carrier subsystem as a standard single-carrier system with a two-tone IMR equal to the M-IMR of the multi-carrier system. For equal power input tones, the multi-tone nature of the signal can be accounted for with a static offset in the OIP3. Using the effective OIP3 from (5) and applying the same formula as is used in (1) to the entire system yields

$$\frac{1}{OIP3_{MWC}} = \frac{1}{OIP3_{Subsystem} - \frac{C.F.}{2}} + \frac{1}{OIP3_{LPF}} + \frac{1}{OIP3_{VGA}} \quad (6)$$

Following the analysis of [3] we then take the two-tone IMR of the entire system (after accounting for the multi-carrier subsystem) as a reasonable proxy for the SNDR at high input signal levels. The MWC reasonably requires 15 dB of SNR in its detection mode to correctly identify the spectral support [2]. Combining this with the cascaded gain of the system results in the maximum allowable input power

$$P_{in,max} \leq OIP3_{MWC} - \frac{SNDR}{2} - G_{system} \quad (7)$$

By accounting for the wideband subsystem separately, the linearity requirements for all of the single carrier system components are relaxed significantly.

4. HYPOTHETICAL SYSTEM

In an effort to further determine the feasibility of the MWC, we now propose a thought experiment wherein a reasonable prototype is assembled from independently developed components.

Our hypothetical system is depicted in Fig. 5. It will require two sets of filters: an input band-pass filter designed to remove out-of-band blockers, and an anti-aliasing low-pass filter to remove unwanted mixing components before sampling. For simplicity our hypothetical system implements both of these system blocks using filters comprised of ideal passive components. The noise floor and distortion ceiling of modern radio receivers are not normally limited by their filters, which makes our use of ideal passive filters reasonable. Ideal passive filters exhibit gain, noise factor, and OIP3 of 0.5, 2, and infinity, respectively.

Immediately following the out-of-band blocking filter is the LNA, whose purpose is to sufficiently amplify the signal so that the additional noise contributions of subsequent system components do not seriously affect the noise floor of the entire system. The MWC places special requirements on the linearity of the LNA because the wide-band, multi-carrier nature of the signal before the second filter is distortion prone. For our hypothetical

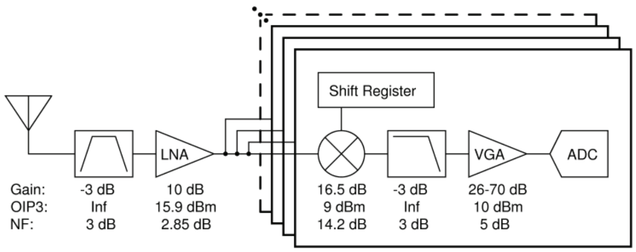

Fig. 5: Our hypothetical MWC system. The system parameters are either established from the literature or are reasonable for the system.

system, we adopt the LNA presented in [8], which has a gain of 10 dB, a noise figure of 2.85 dB, and an OIP3 of 15.9 dBm.

The signal output of the LNA drives the RF port of the mixer. The mixer also sees the wide-band, multi-carrier signal before it is effectively filtered, and it is also distortion prone. We therefore adopt the highly-linear mixer from the same system as our proposed LNA [8]. The mixer has a voltage gain of 16.5 dB, a double-sideband noise figure of 14.2 dB, and an OIP3 of 9 dBm.

In our hypothetical system, we do not specify a design for the VGA or ADC since the system requirements for these components are easily met. For our calculations we assume a minimum voltage gain for the VGA of 26 dB, a noise figure of 5 dB, and an OIP3 of 10 dBm.

We calculated the noise factor of the entire system with Frii's formula (8), which yields a system noise figure of 9.58 dB.

$$Noise\ Factor = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \quad (8)$$

With the entire system specified, we compute and compare the system specifications to those of an LTE receiver. For the high input power distortion limit we assume our multi-carrier signal to consist of ten equal-power, spectrally-adjacent signals. This is the same assumption made in [3] and represents a reasonable case for the MWC. The in-band blocker rejection is taken as the minimum SFDR of a three-level mixing sequence driven with a digital clock running at 4 GHz. The results are summarized in Table 1.

5. CONCLUSION

The specifications depicted in Table 1, represent the most difficult specifications for the MWC. The MWC can compete with traditional LTE receivers in some of these specifications as well as most of the rest of the LTE specifications [4]. The proposed system is very far from meeting the in-band blocking and sensitivity specifications with the proposed architecture.

Even though the performance metrics of the MWC are lower than current radio standards, the MWC offers unprecedented flexibility and, therefore, merits further research.

System:	**Hypothetical MWC**	**LTE Receiver**
Band Selection Range	699-915 MHz	699-2620 MHz
Channel Bandwidth	1.4-20 MHz	1.4-20 MHz
In-Band Blocker Rejection	13.5 dB (reception mode)	64 dB
Input Distortion Limit	-26.6 dBm	-25 dBm
Input Sensitivity	-66.1 dBm (detection mode)	-101.7 dBm

Table 1: Table of system specifications for our hypothetical system and for an LTE receiver

6. REFERENCES

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