DIGITAL COMPENSATION OF SAMPLING INSTANT ERRORS IN THE TRACK-AND-HOLD PORTION OF AN ADC

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ABSTRACT

Track-and-hold (TH) circuits in the front end of high-speed high-resolution analog-to-digital converters (ADCs) typically limit ADC performance at high input signal frequencies. This paper develops mathematical models for THs implemented in both bipolar and MOS technologies. The models are derived by analyzing the sampling instant error and reveal that the nonlinear behavior is dependent on the input signal and it's derivatives. A digital post compensation method is then presented with it's coefficients estimated using an energy-free method in a background calibration configuration. Simulation results on a nonlinear TH model show that the proposed method achieves a significant improvement in the spurious free dynamic range (SFDR). The method is also applied to a commercially available ADC to demonstrate it's effectiveness.

Index Terms— analog-to-digital converter (ADC), trackand-hold (TH), nonlinear, sampling instant error, digital compensation

1. INTRODUCTION

High-performance ADCs are essential components for a wide range of applications in wired and wireless communication, audio and video processing and instrumentation. Sampling rates in excess of 200 MHz and resolutions of greater than 10 bits are increasingly necessary to accommodate application requirements. In these situations the ADC linearity at high input frequencies becomes a critical issue. An important component of ADC linearity is the TH. Unfortunately, the TH often suffers from a variety of nonlinearities such as feedthrough, droop, etc. and introduces frequency-dependent errors [1].

Given the importance of the TH to ADC performance, it's desirable to compensate for it's nonlinearity. In the integrated circuit design community, previous efforts for achieving good high frequency linearity have mainly focused on analog approaches. For example, clock bootstrapping is able to reduce the input signal dependency and enhances the SFDR [3]. However, the bootstrap introduces new design issues in terms of matching, noise and the possibility of oxide reliability [3]. Additionally, it suffers from bandwidth limitations in the ac-

tive analog circuitry and performance degrades at high input frequencies.

The continuous scaling of CMOS technology has allowed for the integration of complicated digital algorithms on chip and the use of digital correction methods to compensate for analog circuit nonlinearities in ADCs. The basic approach of digital compensation is to remove the nonlinearities caused by the TH from the digital output of the ADC in order to minimize the TH error over the desired frequency range.

In the past, phase-plane tables and the Volterra series have been proposed to correct for frequency dependent nonlinearities in ADCs [4]. However, the Volterra series becomes very complex as the order of nonlinearity and the memory in the system increases, frequently making it computationally impractical.

Fortunately, using circuit insights, computationally efficient models can be developed which achieve effective nonlinearity compensation. For example, by focusing on the tracking mode nonlinearity and analyzing the input signal dependent switch-on resistance, [5] proposed a simplified model for dynamic errors and [6] constructed a mixed signal model to describe the dual nature of the TH. Both of these models require a significantly smaller number of coefficients than the general form of the Volterra series and demonstrate significant SFDR improvement.

However, relatively little work has been done on creating circuit insightful TH models and deriving the corresponding digital correction methods. As such, this paper develops a nonlinear distortion model for the TH circuit and a digital compensation scheme to correct for it. The distortion mechanism that this paper focuses on is the transition between the tracking and hold modes, i.e., the sampling instant error.

2. TH SAMPLE INSTANT ERROR MODELING

A conceptual TH circuit and its input/output signals are shown in Fig. 1. The circuit operates in two modes: track and hold, with each lasting around half a clock cycle. In the tracking mode, the switch S (controlled by clock CK) is on and the output voltage y(t) tracks the input voltage x(t). In the transition to the hold mode, S turns off and y(t) remains constant until the next sampling period.



Fig. 1. A conceptual model of the TH.

Denote T_s as the clock period. Assuming the TH begins with a track mode, its input and output are related by

$$y(t) = \begin{cases} x(t), & (n-1)T_s < t \le (n-\frac{1}{2})T_s \\ x[(n-\frac{1}{2})T_s], & (n-\frac{1}{2})T_s < t \le nT_s \end{cases}$$
(1)

Assuming that the TH is followed by an ideal ADC core sampling the signal at every T_s , the digital output of the ADC can be written as

$$y(n) \triangleq y(t)|_{t=nT_s} = x \left[(n - 1/2)T_s \right].$$
 (2)

Note that the quantization noise was ignored to simplify the analysis.

In practice, the TH suffers from different distortions, including feedthrough, pedestal error, etc. One of the most critical distortion sources is the sampling instant error. When the TH moves into the hold state, the switch goes to "OFF" during a non-zero amount of time, known as "sampling instant error". Thus, in the presence of a sampling instant error, the TH output is rewritten as

$$y(t) = \begin{cases} x(t), & (n-1)T_s < t \le (n-\frac{1}{2})T_s + \delta_t(n) \\ x[(n-\frac{1}{2})T_s + \delta_t(n)], & (n-\frac{1}{2})T_s + \delta_t(n) < t \le nT_s \end{cases},$$
(3)

where $\delta_t(n)$ denotes the sampling instant error during the n^{th} sampling period and translates into the magnitude error of the TH output.

Correspondingly, the digital output of ADC consists of the ideal value and the distortion generated by the sampling instant error:

$$y(n) = x\left[\left(n - \frac{1}{2}\right)T_s + \delta_t(n)\right] = x(n) + e(n), \qquad (4)$$

where $x(n) \triangleq x[(n-1/2)T_s]$ denotes the desired signal value the TH needs to hold, and e(n) denotes the sampling instant error induced distortion. Using a Taylor series expansion, the distortion e(n) can be expressed as

$$e(n) = \sum_{i=1}^{\infty} \frac{[\delta_t(n)]^{(i)}}{i!} x^{(i)}(n),$$
(5)

where the i^{th} -order derivative is

$$x^{(i)}(n) = \left. \frac{d^{i}x(t)}{dt^{i}} \right|_{t=(n-1/2)T_{s}}.$$
(6)

Unfortunately, the non-ideal sampling instant is modulated by the input signal and creates nonuniform sampling and harmonics, i.e., $\delta_t(n)$ depends on the TH input signal x(t). In the following sections, two different TH circuits are considered and models for $\delta_t(n)$ and e(n) are derived.

The order of the Taylor expansion is determined by the nonlinearity order that the system needs to capture. For the remainder of the paper, nonlinearities will be modeled up to the third order, since the 2^{nd} - and 3^{rd} -order harmonics are most commonly seen in ADC circuit designs.

2.1. MOS TH

A MOS transistor can be used as an analog switch with its gate voltage (clock) controlling the resistance between the source and drain as shown in Fig. 2 (a). Since the MOS switch only turns off when the gate-source voltage has fallen below the threshold V_{TH} , the time at which the device turns off, i.e., when the TH enters hold mode, depends on the instantaneous level of the input.



Fig. 2. (a) MOS TH circuit and (b) sampling instant error.

As illustrated in Fig. 2 (b), the signal-dependent sampling instant introduces harmonic distortion and becomes noticeable when the clock transition rate is comparable with the input signal slew rate. Suppose that the input signal x(t) is smooth. Let the gate swing between V_c and 0, and have a finite-slope falling edge with a transition period of T_{ct} . The falling edge of the clock can be expressed as

$$V_G(t) = V_c - \frac{V_c}{T_{ct}}(t - nT_s).$$
 (7)

The goal is to sample the input at time nT_s . However, the actual sampling occurs at $nT_s + \delta_t(n)$ when

$$V_G[n+\delta_t(n)] - x[n+\delta_t(n)] = V_{TH}.$$
(8)

Using the 1^{st} -order Taylor series approximation and combining (4), (5), (7) and (8), the sampling instant error becomes

$$\delta_t(n) = \frac{V_c - V_{TH} - x(n)}{\frac{V_c}{T_{ct}} + x'(n)} \\\approx \left[V_c - V_{TH} - x(n)\right] \frac{T_{ct}}{V_c} \left[1 - \frac{T_{ct}}{V_c}x'(n)\right], \quad (9)$$

and the corresponding distortion is

$$e(n) = [V_c - V_{TH} - x(n)] \frac{T_{ct}}{V_c} \left[1 - \frac{T_{ct}}{V_c} x'(n) \right] x'(n).$$
(10)

2.2. Bipolar TH

Semiconductor diodes exhibit a small on-resistance, large offresistance and high-speed switching, thus making them well suited for use as a switch in a TH circuit. A simplified diagram of a TH using a diode bridge is shown in Fig. 3 (a). The diode bridge is turned on and off by switching the current source I(t).



Fig. 3. (a) Bipolar TH circuit and (b) sampling instant error.

Similar to the MOS TH, the sampling instant of the bipolar TH is also input signal dependent due to the non-zero transition time of the current source as shown in Fig. 3 (b). Let the current source I(t) swing between I_o and 0 and have a finite-slope falling edge with transition period T_{ct} . Because the input signal draws a small current Cdx(t)/dt from the top node of the diode bridge, the TH enters hold mode when

$$I(t) = C \frac{dx(t)}{dt}.$$
(11)

Thus, the sampling instant error is obtained as

$$\delta_t(n) = -\frac{T_{ct}}{I_o} C x'(n). \tag{12}$$

Using the 2^{nd} -order Taylor series expansion in (5), the distortion can be written as

$$e(n) = -\frac{T_{ct}}{I_o} C \left[x'(n) \right]^2 + \frac{1}{2} \left(\frac{T_{ct}}{I_o} C \right)^2 \left[x'(n) \right]^2 x''(n).$$
(13)

3. DIGITAL COMPENSATION OF THE SAMPLE INSTANT ERROR

In this section we propose a digital post correction scheme to compensate for ADC nonlinear distortion generated by the sampling instant error of the TH. As shown in Fig. 4, the ADC consists of a TH analog front-end followed by an ideal



Fig. 4. Digital compensation of sampling instant errors.

ADC core (quantizer). Digital compensation corrects the distortion by subtracting the distortion estimation $\hat{e}(n)$ from the observed signal y(n).

The distortion estimate $\hat{e}(n)$ is estimated from the models in (10) and (13). Usually, the derivative is obtained by passing the digital signal through a FIR filter. To increase the estimation accuracy, the signal can be upsampled before FIR filtering.

For cases where the ADC operates in higher Nyquist zones, upsampling the signal to the desired Nyquist zone is required for derivative estimation. Without loss of generality, considering upsampling the signal by a ratio of M. The derivative of the signal can be estimated as

$$x'(n) = \sum_{i=-L}^{L} a_i x\left(n - \frac{i}{M}\right), \qquad (14)$$

where a_i denotes the FIR filter coefficients.

Using differential circuit designs, even order harmonics are usually negligible in ADCs. Focusing only on 3^{rd} -order harmonics and combining with (14), (10) and (13) can be rewritten as

$$e(n) = \sum_{i=-L}^{L} \sum_{j=-L}^{L} h_{ij} x(n) x\left(n - \frac{i}{M}\right) x\left(n - \frac{j}{M}\right)$$
(15)

and

$$e(n) = \sum_{i=-L}^{L} \sum_{j=-L}^{L} \sum_{k=-2L}^{2L} h_{ijk} x \left(n - \frac{i}{M} \right) x \left(n - \frac{j}{M} \right) x \left(n - \frac{k}{M} \right),$$
(16)

respectively, where h_{ij} and h_{ijk} are model coefficients which incorporate both the circuit parameters and the derivative estimation filter coefficients.

The model coefficients can be obtained by either least squares (LS) solutions from training signals in a foreground manner or a background blind estimation approach such as the energy-free method [7].

Once the model coefficients are obtained, the nonlinear distortion can be estimated and subtracted from the ADC output. Because the input signal x(n) is not available, $\hat{e}(n)$ is estimated by replacing x(n) with the observed signal y(n), which has the drawback of degrading the nonlinearity compensation. However, as shown below, the proposed method can still achieve significant linearity improvement.

4. RESULTS

The performance of the proposed method was assessed via computer simulations. An ADC with a Nyquist rate of 100 MHz was simulated. The ADC consists of a TH analog front end followed by a 16-bit quantizer. TH nonlinear distortion is generated using both (10) and (13) with the coefficients V_{ct}/T_c and $T_{ct}C/I_o$ set to 1.41×10^{-2} .

Consider the case where the ADC operates in the 3^{rd} Nyquist zone and a bandpass filtered version of a white Gaussian noise in the 3^{rd} Nyquist zone is used as the training signal. For derivative estimation the FIR filter length parameter L is selected to 1 and the oversampling ratio is set to 2, which results in a total number of coefficients of 6 for the MOS TH and 22 for the bipolar TH.

The energy-free technique is employed to estimate the model coefficients. Fig. 5 shows SFDR plots versus input frequency in the 3^{rd} Nyquist zone of the ADC before and after digital compensation. As can be seen, the SFDR is improved by 10 to 20 dB in these frequencies.



Fig. 5. SFDR before and after compensation: (a) MOS TH, (b) bipolar TH.

The proposed algorithm was also applied to a test chip of a commercially designed 16-bit, 125-MS/s ADC. The digital correction algorithm was applied to the ADC output to compensate for the dynamic nonlinearity generated at its frontend. Fig. 6 shows SFDR versus tone frequency swept across the 5th Nyquist zone of the ADC. The SFDR was improved by 5 to 10 dB in these frequencies.

5. CONCLUSIONS

This paper proposed a digital compensation method to correct for sampling instant errors in TH circuits in high performance ADCs. The TH circuits used in both MOS and bipolar technologies were examined and the resulting models show that the nonlinear sampling-instant error depends on both the TH input signal and its derivatives. The number of coefficients required in the model is relatively small compared to the general form of the Volterra series. The coefficients were estimated using an energy-free technique in a background calibration manner and simulations were presented which demonstrated significant SFDR improvements.



Fig. 6. Measured SFDR in the 5^{th} Nyquist zone.

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