System-driven Metrics for the Design and Adaptation of Analog to Digital Converters

Rajan Narasimha*, Georg Zeitler§, Naresh Shanbhag‡, Andrew C. Singer‡, and Gerhard Kramer§
*Texas Instruments, ln.rajan@ti.com
§Inst. for Communications Engineering, Technische Universität München, Germany, {georg.zeitler,gerhard.kramer}@tum.de
‡Dept. Electrical and Computer Engineering, University of Illinois at Urbana Champaign, {shanbhag,acsinger}@illinois.edu

***Abstract*—In this paper, we review some recent advances in the design of ADCs that exploit system-driven metrics, such as the bit-error rate in a communication link, or mutual information in a scheme employing forward error correction. We show, for example, that ADCs can be designed that maximize the information rate between the quantized output of the channel and the input to the channel for communication links with intersymbol-interference and additive noise. These ADCs dramatically outperform (in terms of achievable information rates) traditional ADC design methods that are based on fixed uniform quantization. Architectures are also developed for ADCs such that system-metrics can be used to dynamically adapt the structure of the ADC to optimize application meaningful criteria, such as bit-error rate for communication over intersymbol interference links.**

I. Introduction

Analog-to-digital converters (ADCs) form the heart of the front-end of many signal processing systems, spanning such applications as communication links, sensor networks, remote sensing, and biomedical applications. For decades, the design of such systems has been driven by metrics that permit system-agnostic designs to be created and refined that enable circuit designers to proceed with the design of an ADC unaware of the applications for which they will ultimately be used. As a result, metrics such as spurious free dynamic range (SFDR) and total harmonic distortion (THD) tend to drive design decisions that often lead to orders of magnitude more complexity and power consumption in the analog front-end than is necessary. In high-speed systems (e.g., in excess of 10 Gb/s), low-power ADCs are particularly difficult to design, and the effective number of bits (ENOB) usually does not exceed $4-6$ [1]–[3].

In this paper, we review recent advances in the design of ADCs that employ system-metrics to configure ADC design parameters. Specifically, we present two techniques for ADC design in communication links with intersymbol-interference and additive noise (Fig. 1): (a) maximize the information rate (IR) between the quantized channel output and the channel input (Section III), and (b) ADC-design to minimize the bit error-rate (BER) (Section IV). The IR-maximizing ADC gives a bound on achievable performance in a link with error correction, whereas the BER-optimal ADC presents a practical technique to approaching this bound. Further, we demonstrate a BER-optimal ADC in concert with both a tapped-delay line linear equalizer and look-up table (LUT)-based detector. Finite precision analysis demonstrates that LUT-based detectors actually reduce digital post-processing power and area up to $75\,\%$ in a 45 nm CMOS process. Additionally, an adaptive, approximate minimum BER algorithm that can determine the BER-optimal reference levels for high-speed links employing a flash ADC architecture is presented.

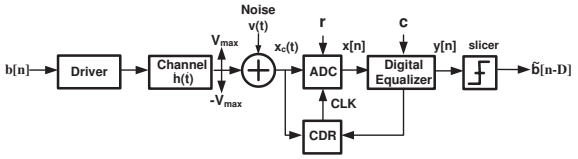


Fig. 1. Role of an ADC in a communication link with intersymbol-interference and additive noise.

II. System Model

We consider digital transmission over a discrete-time channel with intersymbol interference (ISI) and additive white Gaussian noise (AWGN), such that the channel output is

$$X_c[n] = \sum_{i=0}^{M-1} h[i]B[n-i] + V[n], \quad n = 1, 2, \ldots, k, \quad (1)$$

where the input bits $B[n] \in \{\pm 1\}$ are equally likely, independent, and identically distributed (i.i.d.). The channel has M fixed real coefficients $h[i]$, and we define the state of the channel as $S[n] = B_{n-M+2}^{n}$, where B_{n-M+2}^{n} is the sequence $\{B[n-M+2], B[n-M+3], \ldots, B[n]\}$. The noise $V[n] \sim \mathcal{N}(0, \sigma^2)$ satisfies $\mathrm{E}[V[n]V[n']] = \sigma^2\delta_{nn'}$, and the signal-to-noise ratio (SNR) is defined as $\mathrm{SNR} = \sum_{i=0}^{M-1} h^2[i]/\sigma^2$. At the receiver, the channel output $X_c[n]$ is quantized using an ADC, modeled as scalar quantization with N quantization regions. Employing a quantization function $Q_1 : \mathbb{R} \to \mathcal{X}$, where $\mathcal{X} = \{0, 1, \ldots, N-1\}$ is the finite set of quantization indices, we have that $X[n] = Q_1(X_c[n])$ is the quantizer output. Throughout, it is assumed that the receiver has perfect channel state information, and we refer to [4] for the channel estimation problem with low-precision ADCs.

III. Maximum Information Rate ADCs

The information rate of the ISI channel (1) combined with scalar quantization is defined as (cf. [5, Theorem 4.6.4])

$$\begin{aligned} I(B; Q_1(X_c)) &= \lim_{k\to\infty} \frac{1}{k} I(B^k; X^k | S[0]) \quad (2) \\ &= \lim_{k\to\infty} \frac{1}{k} \left[H(X^k|S[0]) - H(X^k|B^k, S[0]) \right]. \end{aligned}$$

TABLE I
SCALAR SINGLE-BIT ($N = 2$) ADCS FOR $\boldsymbol{h} = [0.5, 0.707, 0.5]^{\mathrm{T}}$, $K = 2$.

SNR	Threshold(s)	Region indices	$I(B; Q_1(X_c))$
3 dB	0	$[0, 1]$	0.355
7 dB	0	$[0, 1]$	0.498
11 dB	$[-1.28, 0, 1.28]$	$[0, 1, 0, 1]$	0.672
18 dB	$[-1.22, 0, 1.22]$	$[0, 1, 0, 1]$	0.980

Here, X^k denotes the sequence $\{X[1], \ldots, X[k]\}$. For a fixed channel and a fixed quantizer, the entropy $H(X^k|S[0])$ can be computed efficiently with the forward recursions of the BCJR-algorithm on the trellis of the channel [6], and $H(X^k|B^k, S[0]) = k\, H(X[1]|B[1], S[0])$ can be calculated using Q_1. Consequently, the information-rate maximizing quantization function with N quantization regions can be found by solving

$$\sup_{Q_1:\mathbb{R}\to\mathcal{X}} I(B; Q_1(X_c)) \quad \text{s.t.} \quad |\mathcal{X}| = N, \tag{3}$$

which seems hard to solve since k tends to infinity in (2), and since (3) is a functional optimization over the quantization function Q_1. We therefore solve an approximation of (3) by lower bounding $I(B; Q_1(X_c))$ for $K = \{0, 1, 2, \ldots\}$ as [7, Lemma 1]

$$I(B; Q_1(X_c)) \geq \lim_{k\to\infty} \frac{1}{k} \sum_{i=1}^{k} I(B[i]; X_i^{i+K} | B_{i-M+1}^{i-1}), \tag{4}$$

and by discretizing the continuous observation $X_c[i]$ at high resolution, yielding the discrete variable $\bar{X}_c[i] \in \bar{\mathcal{X}}$. With $\bar{X}[i] = \bar{Q}_1(\bar{X}_c[i])$, an approximation of (3) becomes

$$\bar{I}^* = \max_{\bar{Q}_1:\bar{\mathcal{X}}\to\mathcal{X}} I(B[i]; \bar{X}_i^{i+K} | B_{i-M+1}^{i-1}) \quad \text{s.t. } |\mathcal{X}| = N, \tag{5}$$

which we solve with an iterative algorithm [7] that can be viewed as a modification of the information bottleneck iterative algorithm [8].

As an example of such an optimization, suppose the channel is $\boldsymbol{h} = [h[0], h[1], h[2]]^{\mathrm{T}} = [0.5, 0.707, 0.5]^{\mathrm{T}}$ [9]. Table I summarizes the characteristics of 1-bit/sample ($N = 2$) quantizers for various SNRs obtained from our iterative quantizer design algorithm for $K = 2$. Evidently, at low SNR, the optimal single-bit quantizer for that channel has a single threshold at zero (and is therefore equivalent to a simple slicer). At high SNR, however, such a slicer is suboptimal, and is outperformed by a single-bit quantizer with discontiguous quantization regions. The advantage from information rate optimized quantization is further illustrated in Fig. 2, where we show information rates versus the SNR for the same channel. Here, the gain from optimized quantization is most pronounced at high SNR, since the information rate of the slicer saturates at about 0.76, while an information rate of 1 can be achieved with optimized single-bit quantization at high SNR.

IV. BER OPTIMAL ADC: DESIGN

Turning to quantization based on a detection criterion, we represent the quantizer output using N levels $\mathbf{r}=[r_1, \ldots, r_N]^{\mathrm{T}}$ defined by $N-1$ thresholds $\mathbf{t} = [t_1, \ldots, t_{N-1}]^{\mathrm{T}}$, non-

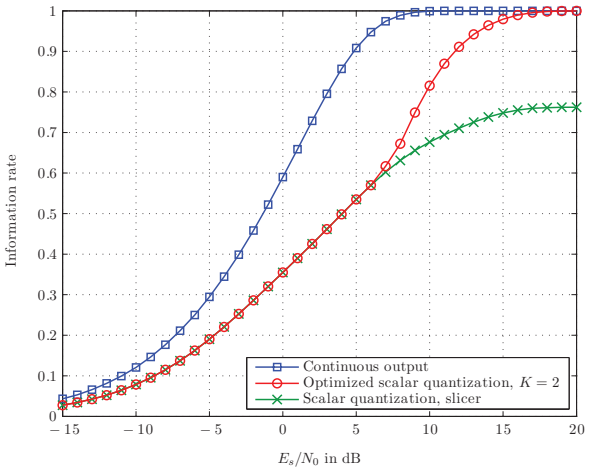


Fig. 2. Rates for $\boldsymbol{h} = [0.5, 0.707, 0.5]^{\mathrm{T}}$; all quantizers have 1 bit/sample.

uniformly spaced, using a BER metric. In the system presented in Fig. 1, the equalizer output $\tilde{b}[n]$ is given by

$$\tilde{b}[n] = \mathrm{sgn}(y[n]) = \mathrm{sgn}\left(\sum_{j=0}^{L-1} c[j]x[n-j]\right). \tag{6}$$

An error is made when $\tilde{b}[n] \neq b[n]$ (assuming $D = 0$), so the BER is computed by averaging over all possible values of $y[n]$, and hence all vectors $\mathbf{x}_n = [x[n], x[n-1], ..., x[n-L+1]]^{\mathrm{T}}$ such that $\tilde{b}[n]$ produces an error at the slicer:

$$\begin{aligned} \mathrm{BER} &= \mathbb{P}\{b[n] \neq \tilde{b}[n]\} \\ &= \sum_{y[n]} \left[\mathbb{P}\{y[n]\} \frac{1}{2}\left(1 - b[n]\tilde{b}[n]\right)\right] \\ &= \sum_{\mathbf{x}_n} \left(\prod_{j=0}^{L-1} \mathbb{P}\{x[n-j] = r_k\}\right) \frac{1}{2}\left(1 - b[n]\tilde{b}[n]\right), \end{aligned} \tag{7}$$

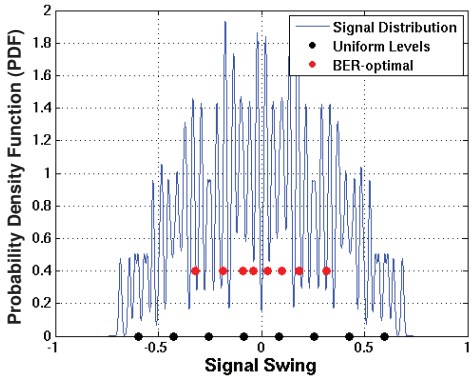
where $\mathbb{P}\{x[n-j] = r_k\}$ is given by

$$Q\left(\frac{t_{k-1} - z[n-j]}{\sigma}\right) - Q\left(\frac{t_k - z[n-j]}{\sigma}\right), \tag{8}$$

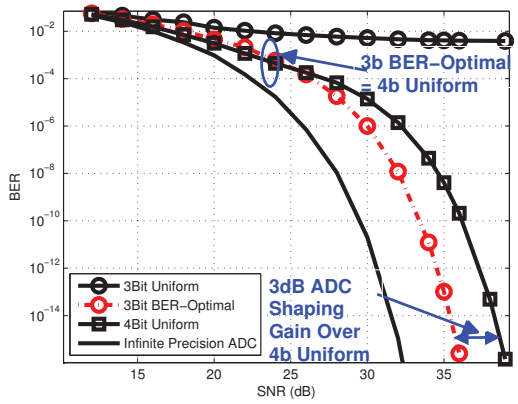
$\mathbb{P}\{\bullet\}$ signifies the probability of an event, and $Q(\bullet)$ is the Gaussian Q-function. A BER-optimal ADC is one where $\mathbf{r}$ and $\mathbf{t}$ are chosen to minimize (7).

A closed form expression for the BER optimal parameters of the ADC, $\mathbf{r}$ and $\mathbf{t}$, is difficult to obtain due to the highly non-linear objective function. Therefore, we employ a gradient descent technique to determine the parameters. The following update equations are used to compute $\mathbf{r}$ iteratively. For the i-th iteration of the algorithm, we have

$$\begin{aligned} \mathrm{BER} &= f(\mathbf{h}, \mathbf{r}, \mathbf{t}, \mathbf{c}, \sigma) \\ \mathbf{r_i} &= \mathbf{r_{i-1}} + \mu \left(\frac{\partial\ \mathrm{BER}}{\partial \mathbf{r}}\right)\Bigg|_{\mathbf{r}=\mathbf{r_{i-1}}} \\ &\approx \mathbf{r_{i-1}} + \mu \left(\frac{\Delta\ \mathrm{BER}}{\Delta \mathbf{r}}\right) \end{aligned} \tag{9}$$



(a)



(b)

Fig. 3. Performance for a high-ISI channel employing 2-PAM modulation and a LE: a) received signal distribution and ADC output levels for a high-ISI channel, and b) BER vs. SNR curves for a 3-bit uniform, 3-bit BER-optimal, 4-bit uniform, and an infinite-precision ADC, respectively.

$$t_{k,opt} = \frac{r_{k,opt} + r_{k+1,opt}}{2}. \tag{10}$$

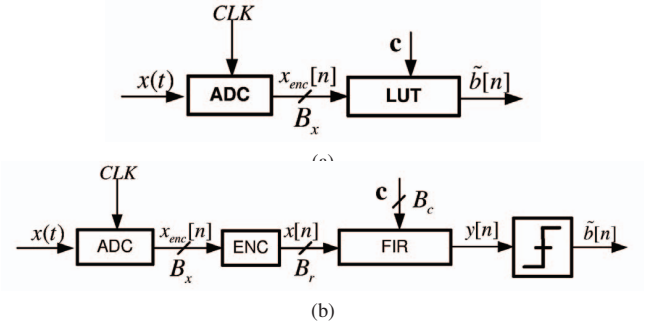
The placement of $\mathbf{t}$ remains given by (10), where $r_{k,opt}$ denotes the optimum k-th reference level obtained through the iteration (9). To avoid differentiating the sign function, the gradient is approximated by finite differences [10].

This algorithm can be extended for decision-feedback equalizers by replacing the right-hand side of (6) with

$$\operatorname{sgn}\left(\sum_{j=0}^{L-1} c[j]x[n-j] - \sum_{l=1}^{L_2} d[l]\tilde{b}[n-D-l]\right).$$

A. Simulation Results

We now review simulation results comparing a uniform ADC and a BER-optimal ADC for a 20" FR-4 channel carrying 10 Gb/s data and employing linear equalization ([11] also includes a comparison with Lloyd-Max quantization). The received signal distribution and ADC output levels at 32 dB SNR are shown in Fig. 3(a). We observe that the 3-bit BER-optimal ADC is significantly better than the 3-bit uniform ADC as shown in Fig. 3(b). In this case, performance of the



(b)

Fig. 4. Two equalization techniques: a) LUT-based non-linear, and b) linear equalizer (LE).

3-bit uniform ADC does not improve with increasing SNR due to quantization noise. Compared to a 3-bit uniform ADC, a shaping gain S_G is too large to be quantified; compared to a 4-bit uniform ADC, $S_G(\text{BER} = 10^{-15}) = 3\,\text{dB}$. In the next section, we compare two architectures to implement the equalizer that follows the BER-optimal ADC.

B. Fixed Equalizer Architectures for BER-aware ADC

The representation of the ADC output values is tied to the implementation of the equalizer. Since the quantization levels are no longer uniform, changes in the digital output correspond to different changes in the input. An equalizer employing linear operators cannot operate directly on such digital outputs. To address this issue, two equalizer architectures are considered (cf. Fig. 4): a) a look-up table-based [11], and b) a tapped-delay line linear equalizer (LE). The LUT-based equalizer operates directly on the L ADC samples, $x_{enc}[k]$, each represented with B_x bits, in order to make the decision $\tilde{b}[k]$. The tapped-delay line LE first maps $x_{enc}[k]$ to $x[k]$ with B_r bits ($B_r > B_x$), so that the mapping $x(t) \mapsto x[k]$ is closer to linear.

We now compare the complexities of the two detection techniques following the BER-optimal ADC proposed in Fig. 4. Both architectures were synthesized using Nangate's 45 nm cell library [11]–[13]. For the channel with receive signal distribution shown in Fig. 3(a), two design points in the plots, corresponding to 24 and 32 dB SNR are synthesized and compared. From Table II, which presents area and power estimates, we see that the LUT-based equalizer is in fact much simpler than the tapped delay-line LE, indicating BER-optimal ADCs can be realized with minimal complexity impact. At low SNR for the ISI channel considered, the detector architecture based on the tapped delay-line LE occupies 360 μm^2, while the area of the LUT-based equalizer is only 100 μm^2. This represents an area reduction of 74 %. Detector power consumption reduces from 82 μW to about 27 μW, representing a 67 % reduction. For high SNR, area and power reduce by 76 % and 73 %, respectively. A global voltage of 0.95 V and operating clock frequency of 400 MHz were used in this evaluation.

V. Adaptive Minimum BER ADC Reference Level Algorithm (AMBER-ADC)

In this section, we develop the AMBER algorithm for adapting ADC reference levels, analogous to the development

TABLE II
COMPARING COMPLEXITY OF LUT-BASED EQUALIZER WITH LE.

SNR (dB)	Cell Area (μm^2)	Power (μW)
24 (LUT)	100	27
24 (LE)	360	82
32 (LUT)	100	27
32 (LE)	425	101

of AMBER for equalizer coefficients [14]. The BER, given by (7), is a non-smooth function of $\mathbf{c}$ and $\mathbf{r}$. In order to develop an adaptation algorithm for reference levels, we assume that the equalizer coefficients are fixed at $\mathbf{c}$. The slicer input $y[k]$ and the slicer error $e[k]$ are given by

$$\begin{aligned} y[k] &= \mathbf{c}^{\mathrm{T}}\mathbf{x}[k] \\ e[k] &= b[k] - \sum_{j=0}^{L-1} c[j]x[k-j]. \end{aligned} \tag{11}$$

Therefore,

$$\mathrm{E}[e^2[k]] = \mathrm{E}\left[\left(b[k] - \sum_{j=0}^{L-1} c[j]x[k-j]\right)^2\right]. \tag{12}$$

The gradient of the expected squared error taken with respect to the reference levels can be written as

$$\frac{\partial \mathrm{E}[e^2[k]]}{\partial r_n} = -2\mathrm{E}\left[e[k] \sum_{j\in J_n[k]} c[j]\right], \tag{13}$$

where $J_n[k] = \{j : x[k-j] = r_n\}$. Approximating the gradient of MSE from (13) by its stochastic counterpart and taking the sign of the error $e[k]$, we obtain

$$r_n[k+1] = r_n[k] + \mu_r \operatorname{sgn}(e[k]) \sum_{j\in J_n[k]} c[j], \tag{14}$$

where μ_r is the step-size for the reference level update. The thresholds are updated as

$$t_i = \frac{r_i + r_{i+1}}{2}, \text{ for } i = 1, \ldots, N. \tag{15}$$

Analogous to the method employed for equalizer updates [14], the signed LMS algorithm (14) for ADC reference levels can be modified as follows, to obtain an algorithm for reference levels:

$$r_n[k+1] = r_n[k] + \mu_r I[k] \operatorname{sgn}(e[k]) \sum_{j\in J_n[k]} c[j]. \tag{16}$$

To evaluate the algorithm, the equalizer coefficients are initialized to $\mathbf{c} = \mathbf{c}_{opt}$. In practice, $\mathbf{c}$ can be initialized to $[0, \ldots 0, 1, 0 \ldots 0]^{\mathrm{T}}$, and the coefficients can be updated using either the LMS or AMBER algorithm with the reference levels uniformly spaced. Once the equalizer coefficients converge, the reference levels can then be updated by choosing a small step-size μ_r due to the sensitivity of BER to reference levels. A practical implementation of the algorithm would require a high resolution DAC for the comparator thresholds. A grid of initial conditions was explored, and the best performance gains quantified. Fig. 5 compares the BER calculated using AMBER and the optimal reference level settings for a 3-bit BER-optimal ADC. The reference levels were initially uniformly spaced spanning half the dynamic range, i.e, $-V_{max}/2$ to $V_{max}/2$. The BER was evaluated after 4×10^5 bit periods. Fig. 5 demonstrates that AMBER achieves the shaping gains predicted in Fig. 3(b) (cf. [11]). We carried out simulations up to an SNR of 28 dB to keep the simulation feasible.

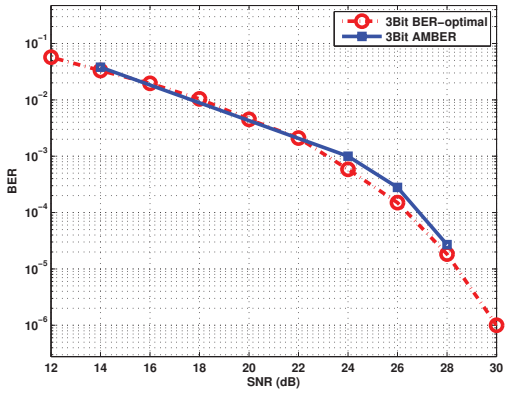


Fig. 5. Performance evaluation of AMBER algorithm for reference level updates.

REFERENCES

[1] H.-M. Bae, J. Ashbrook, J. Park, N. Shanbhag, A. Singer, and S. Chopra, "MLSE receiver for electronic dispersion compensation of OC-192 fiber links," *IEEE Journal of Solid State Circuits*, vol. 41, no. 11, pp. 2541–2554, 2006.

[2] M. Harwood *et al.*, "A 12.5 Gb/s SerDes in 65nm CMOS using a baud-rate ADC with digital RX equalization and clock recovery," in *IEEE International Solid-State Circuits Conference*, 2007.

[3] P. Schvan *et al.*, "A 24GS/s 6b ADC in 90nm CMOS," in *IEEE International Solid-State Circuits Conference*, 2008.

[4] O. Dabeer and U. Madhow, "Channel estimation with low-precision analog-to-digital conversion," in *Proc. IEEE Int. Conf. Comm.*, 2010.

[5] R. G. Gallager, *Information Theory and Reliable Communication*. John Wiley and Sons, Inc., 1968.

[6] D. M. Arnold, H. A. Loeliger, P. O. Vontobel, A. Kavčić, and W. Zeng, "Simulation-based computation of information rates for channels with memory," *IEEE Trans. Inf. Theory*, vol. 52, no. 8, pp. 3498–3508, Aug. 2006.

[7] G. Zeitler, A. C. Singer, and G. Kramer, "Low-precision A/D conversion for maximum information rate in channels with memory," in *Proc. IEEE Int. Symp. on Information Theory*, 2011.

[8] N. Tishby, F. C. Pereira, and W. Bialek, "The information bottleneck method," in *Proc. 37th Ann. Allerton Conf. on Communications, Control, and Computing*, 1999, pp. 368–377.

[9] W. Hirt, "Capacity and information rates of discrete-time channels with memory," Ph.D. dissertation, ETH Zürich, 1988.

[10] William H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes: The Art of Scientific Computing*. NY: Cambridge University Press, 2007.

[11] M. Lu, A.Singer, and N. Shanbhag, "BER-Optimal analog-to-digital converters for communication links," in *International Symposium on Circuits and Systems*, 2010.

[12] Nangate, "45 nm cell library," Website, www.nangate.com/openlibrary/.

[13] R. Narasimha, N. R. Shanbhag, and A. Singer, "Ber-based adaptive adc-equalizer based receiver for communication links," in *IEEE Workshop on Signal Processing Systems*, 2010.

[14] C.-C. Yeh and J. R. Barry, "Adaptive minimum bit-error rate equalization for binary signaling," *IEEE Transactions on Communication*, vol. 48, no. 7, pp. 1226–1235, 2000.