POWER SUPPLY GENERATION AND BATTERY MANAGEMENT FOR ENERGY EFFICIENT SDR

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ABSTRACT

Driven by the always increasing feature's demand of cellular phones, together with the tight constraint of smart power saving, power management (PM) keeps on developing and becoming more complex from one generation to the next. To keep on being competitive at the same time, PM can't be considered as a mere isolated/concentrated device anymore but attention must be turned to a smart partitioning. This is specifically true when extending PM concepts towards Software Defined Radio (SDR) chips. In this paper we give an introduction about stand-alone PMU chips, and then describe challenges to cope with when integrating PM features on a complex SoC.

Index Terms— PMU, LDO, DC-DC, SoC, SDR

1. INTRODUCTION

In portable products such as mobile phones the power-management function is extremely important because it determines the effective battery life, which is an important feature for every end-user. Typically, the power management block will supply different parts of the circuitry at the most appropriate voltage and optimize consumption by trading off speed in the case of digital circuit, and dynamic performance in the case of analog circuits.

For circuit-based power-management features it is not necessary to use the most advanced process in terms of scaling, because these features are essentially analog. Therefore the cost of the features will not follow Moore's law at the same rate as applicable to pure CMOS digital circuits. Further arguments to implement the PMU on a separate chip are issues like special process options including high voltage devices, thick metal to ease power routing and the incorporation of other circuits like the audio amplifier on the PMU chip.

However, good arguments for implementing the power management on a complex SoC are more efficient interactions in between power management and functional units and cost savings due to reduction of number of components. Such power saving versus complexity trade-offs in SoC architectures are shown in Figure 1.

The power management strategy is to provide maximum performance only when needed. To the end-user this should ideally be handled in the background without any need for interaction.

The important design parameters, which determine the digital power consumption are shown in equation (1):

$$Power = \alpha \cdot C_L \cdot V_{dd}^2 \cdot f + I_{leak}(V,T) \cdot V_{dd} \qquad (1)$$

It is important to note that the total power consists of two terms, the "switching power" and the "passive power" which is determined by the leakage currents.

For a low "switching power" design the physical level opportunities are dynamic multi-Vdd management, dynamic multi Vth (by back-gate biasing) management and CLK-gating. Major system level opportunities are the exploitation of parallelism, hardwired co-processors and memory minimization.

The "passive power" is determined by the leakage currents and can be reduced by applying minimum Vdd and disconnecting functional blocks from the supply when they are in standby mode.

Complex and compact mobile systems require a smart partitioning of power management functions (e.g. direct to battery). Intelligent power management systems consist of efficient power generation like programmable switch-mode regulators for low voltage applications. Digital control enables dynamic management of power conversion (wake-up, sleep, interrupt-functions, voltage scaling).

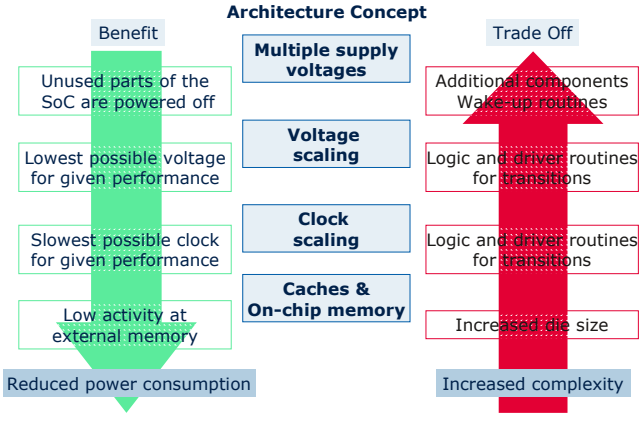

Figure 1: Power Savings in Baseband Processors

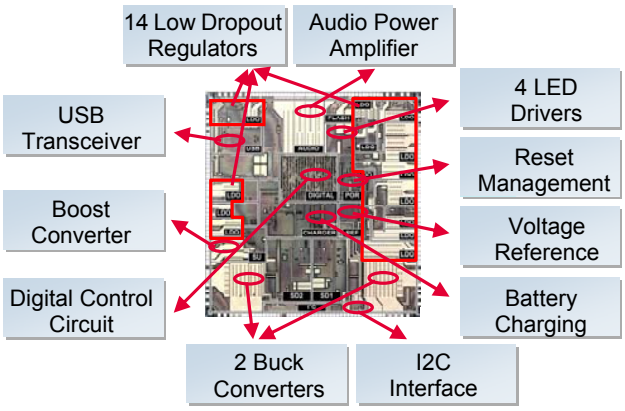

Figure 2: Stand-alone PMU Chip

2. STANDALONE PMU CHIP

In Figure 2 we show an example for a state-of-the-art stand-alone PMU chip. The chip incorporates both analog and digital functionality and is based on a standard quarter micron CMOS process. Special process options like thick metal, double Gox and extended drain devices allow the handling of currents of 1A and voltages of up to 5.5V (Battery) and even up to 15V for the charger.
The following fuctional units are integrated on the chip:

- A range of 16 low dropout regulators (LDOs) depending on the number of functions
- Two Buck converters to control low voltage system circuits
- A boost converter to enable white LED supply
- Battery charging and battery management circuits
- Four LED drivers with PWM outputs
- A USB transceiver and a I2C interface
- A audio power amplifier
- A reset management and digital control circuit

Digital control enables dynamic management of power conversion (wake-up, sleep, interrupt-functions, voltage scaling).
A small package (121 pins including thermal ground pins) minimize board space but demand for thermal management which keeps any heat dissipation issue under control.

3. PMU FOR SYSTEM-ON-CHIP

When integrating power management features on a complex SoC this has quite some consequences on the overall PMU system approach, as well as on the detailed implementation. Compared to the previously described state-of-the-art (standalone PMU chip), an integrated PMU on a large SoC will face the following disadvantages:

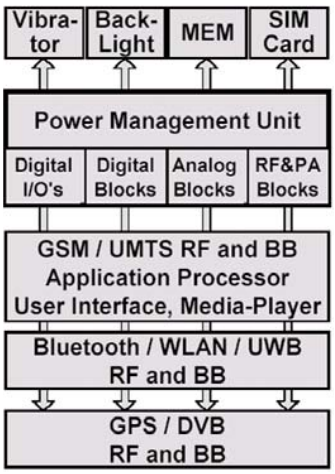

Figure 3: SoC with integrated PMU for Mobile Applications

- Higher relative wafer cost per mm^2 for PMU part due to usage of latest CMOS technology
- No dedicated high-voltage features
- No extra-thick top-level metallization available
- Risk of noise coupling, e.g. between DC-DC converters and RF parts
- Complexity of SoC

On the other hand we can consider the advantages, and careful analysis of both technical and business arguments must be done to decide on what is the overall best solution:

- More efficient digital control algorithms possible
- Shorter routing on-chip, therefore less losses in power routing
- Flexible power management feasible, enabling optimized power consumption for the whole system (for example: switch off any block on the SoC that is not used)
- Smaller form factor
- Package cost

For high-volume SDR chips or any SoCs with usually large digital parts it makes most sense to develop them in the most advanced deep submicron CMOS technologies available. However, such technologies usually show several new effects not present in the standalone PMU chip scenario that have to be considered now. For example one must figure out how to integrate high voltage PMU features like a charger or DC-DC converters in such technologies. Consequently the design of specific devices like high-voltage capable MOS transistors in the technology of choice is a pre-requisite to allow high voltage usage. Furthermore, due to higher leakage currents in these technologies one must find a way to still get low power consumption during sleep and standby modes, but be able to get the full compute power required during active chip operation modes.

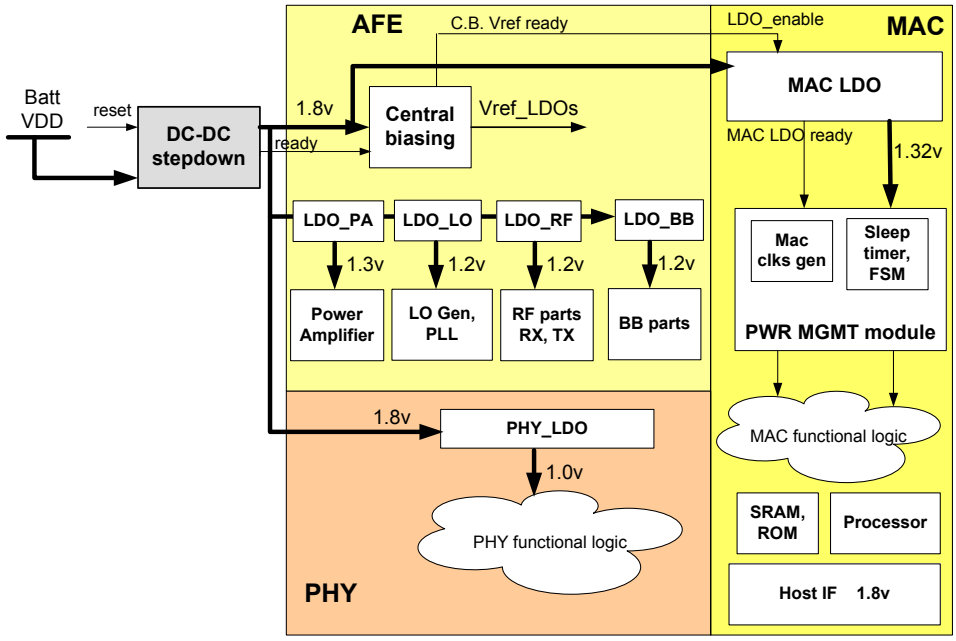

Figure 4: Multiple Power Domains for an UWB SoC

To fully optimize the power consumption of the system there are several measures one can implement on different levels:

1. Separate supply domains for large sub-blocks, having its own LDO or even DC/DC converter. This allows usage of high performance core devices, but still having acceptable leakage during standby modes.
2. Dynamic voltage scaling: Depending on the required compute power and more parameters like process corner and temperature, the supply voltage for specific blocks can be set or regulated to an optimum value.
3. Dynamic frequency scaling: Not only voltage, but also clock frequency can be scaled down during idle modes, where full compute power is not required
4. Adding micro-switches in series to the supply within digital sub-blocks again allows minimization of leakage currents during standby.
5. Analog blocks: Scalability of performance vs. power consumption. For example ADCs can be chosen and designed such that the resolution (number of bits) and/or sampling frequency scales at least partly with current drain.
6. System Level: Several levels of operative modes can be foreseen, from power-off, over deep-sleep towards active modes. This should be defined in an early project state so that all sub-blocks or IP blocks to be integrated can support the power management concept.

The latter one seems to be crucial when thinking about SDR chips. One can imagine that not all blocks will allow performance/power scaling, but there will be many redundant blocks integrated, but most of the time powered off.

Even if the supply voltage level is the same between different blocks, for ESD reasons and due to the fact that the supply on either the sending or receiving side could be disabled, one must take special measures when routing signals from one supply domain to the other. Therefore specific isolation cells between such blocks are required.

4. A CASE STUDY: UWB SOC POWER MANAGEMENT

In this section we give some insight in recent SoC chip developments, focusing on the power management implementation issues.

An example is shown in Figure 4: Multiple Power Domains for an UWB SoC. This SoC consists of three large power domains (MAC, PHY, analog front-end AFE) and several sub-domains. The battery supply of 2.5 to 4.5V is first converted to a single 1.8V supply rail by an external DC-DC step-down power converter. In this case there are two reasons for having this block external: first, the 90nm CMOS technology used did not provide a high-voltage device capable to withstand the battery voltage. Second, due to the wideband nature of the product (UWB) the risk of noise coupling from the DC-DC to the RF section was rated too high. Even with external solution this risk is still there, since spurious tones might couple via the 1.8v supply rail into the RF and analog part. This can be optimized by carefully choosing the external blocking capacitor.

Inside the chip there are dedicated LDOs for the different supply domains. In the digital domain (MAC, PHY) the voltages are chosen to optimize the tradeoff between required maximum operating clock frequency and leakage. Specifically for the processor, the supply voltage can be programmed by switching the feedback resistor inside the LDO block (Figure 5). Each LDO consists of a PMOS pass transistor, a regulation loop with amplifier to control the gate of the PMOS, and a resistive divider to choose the output voltage. An external blocking capacitor is connected to each LDO output voltage, which in combination with internal capacitors filters out transients and thus reduces both the noise level on the internal voltages, as well as noise coupling between different voltage domains.

For the analog and RF blocks the split into different domains is mainly not to allow different voltage levels, but

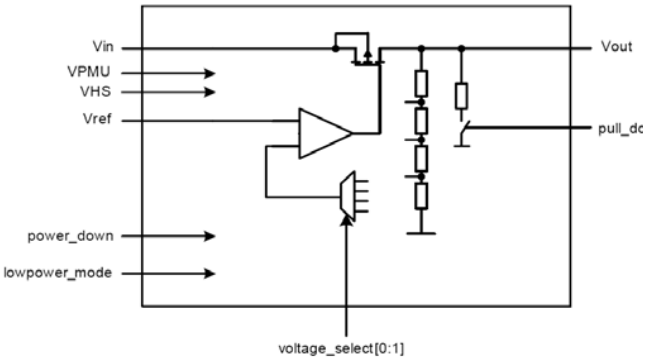

Figure 5: Programmable LDO

again to enhance isolation between the blocks and decouple noise sensitive parts from the rest.

When implementing several supply domains on one silicon die, care must be taken to properly handle digital interfaces between the blocks. When the voltage levels are different between the sending and receiving block, isolation stages must be implemented to convert the levels properly. Additional measures are required when the supply domains can be switched off, which is also true for digital sub-blocks that are disabled by means of micro-switches. How this can be handled is shown in Figure 6.

The overall power management system can become quite complex to handle, as indicated in Figure 7. Several levels of operation modes are required, from power-off over different levels of sleep and idle modes, up to the active modes, where the full compute power is required. Even then some parts of the chip might be in power-down, for example in a system with time duplexing either the RX or the TX part can be switched off. Care must be taken to consider sufficient transition times between on- and off-state.

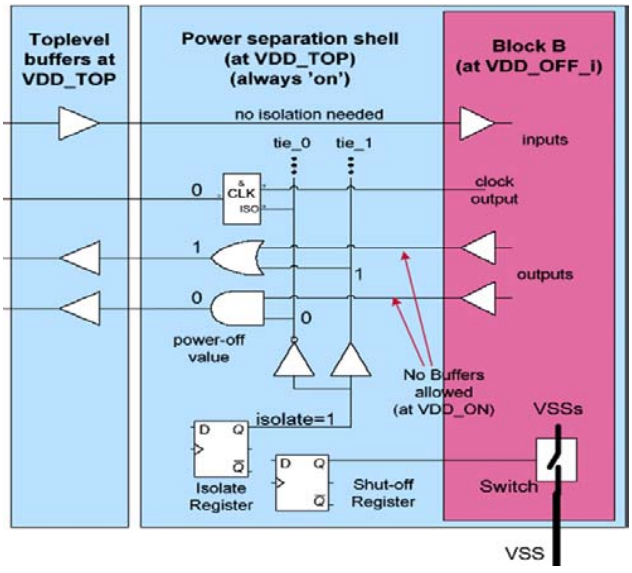

Figure 6: Multi-VDD Block Isolation

5. OUTLOOK

The performance and complexity trends in ICs for mobile multimedia communications and "Software Defined Radio" are further increasing and generate enormous challenges on power management. A further development and optimization of the current concepts of providing maximum performance only when needed is of utmost importance. The concept of power management and reduction by dynamic supply-voltage and threshold-voltage (through backbias) scaling has to be further optimized and adapted to new process technologies. Beyond of that, in the future even more efficient and cheaper concepts have to be explored, like capacitor-less LDOs or DC-DC converters with integrated inductors.

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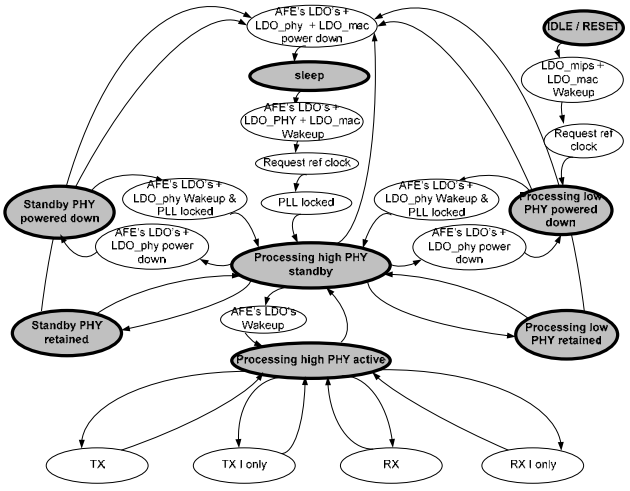

Figure 7: State Diagram of System Power States