DESIGN OF BLOCK-STRUCTURED LDPC CODES FOR ITERATIVE RECEIVERS WITH SOFT SPHERE DETECTION

Predrag Radosavljevic and Joseph R. Cavallaro

Department of Electrical and Computer Engineering
Rice University, Houston, TX 77005, USA
{rpredrag, cavallar}@rice.edu

ABSTRACT

In this paper we design block-structured LDPC codes for iterative MIMO receivers with soft sphere detection in particular channel environments. The receiver EXIT charts are used as a design tool. The main design constraint is to preserve the block-structure of parity-check matrices supporting modular semi-parallel decoder architectures. We show that newly designed block-structured code profiles provide improved error-rate performance of between 0.5 dB and 1 dB in different channel environments for moderate codeword size.

Index Terms– low-density parity-check (LDPC) codes, iterative receivers, extrinsic information transfer (EXIT) functions, code design, performance analysis

1. INTRODUCTION

Iterative detection-decoding is a known receiver technique which provides promising error-rate performance in multiple input multiple output (MIMO) wireless systems. In this work we assume inner bounded soft sphere detection (BSSD) from [1], and outer decoding supported by the block-structured LDPC codes such as codes from [2, 3]. The error rate performance improvement can be achieved by increasing the sphere radius and/or by increasing the decoder codeword size. But, detection throughput becomes smaller and/or decoder area is larger. On the other hand, as shown in [4], the error-rate performance of the iterative receiver can be improved without additional implementation cost by designing LDPC codes for a particular inner detector and channel environment.

Richardson *et al.* developed the density evolution (DE) algorithm for designing capacity approaching LDPC codes [5]. To reduce the computational complexity of the DE algorithm, Gaussian approximation (GA) of reliability messages is often applied. In this case, mutual information between messages and corresponding bits is determined directly from the variance. The extrinsic information transfer (EXIT) functions of variable-node and check-node decoders (sub-blocks of LDPC decoder) characterize transfer of the *a priori* mutual information at the decoder input into extrinsic mutual information at the decoder output. The EXIT chart analysis is a convenient tool for designing excellent codes, as shown in [4] for fully random code profiles. Optimization of fully random codes using EXIT charts is typically considered in the literature [6, 7, 8]. On the other hand, the code-design constraint applied in this work is to preserve the block-structure of irregular parity-check matrices (PCMs). These matrices provide excellent error-correcting performance close to random codes, and modular semi-parallel decoder architectures are supported where a single structured processor core supports multiple code rates and codeword sizes [9, 3]. Also, a single structured decoder can be utilized in different channel environments for which different block-structured code profiles are designed and optimized. Original block-structured LDPC codes, for example ones that are proposed for IEEE 802.11n standard [2], are designed with no consideration of any specific detector and/or iterative feedback from decoder to detector. Therefore, there is a potential to significantly improve error rate performance if the code profile is designed for a specific soft detector and a particular channel environment.

The paper is organized as follows. In Section 2 the principles for designing the LDPC codes using EXIT charts are reviewed. Design of block-structured LDPC codes in Rayleigh and Winner channels [10] is described in Section 3 and Section 4, respectively. The frame error-rate performance improvement of newly designed block-structured LDPC code profiles with finite codeword length is shown in Section 5. The paper is concluded in Section 6.

2. DESIGN OF LDPC CODES FOR ITERATIVE DETECTION-DECODING WITH EXIT CHARTS

The interface between soft sphere detector (SSD) and LDPC decoder is shown in Fig. 1. Reliability messages are iteratively passed between the variable-node decoder (VND) and check-node decoder (CND), as well as between VND and SSD blocks. The *a priori* mutual information I_A of a particular block represents average mutual information between *a priori* messages and corresponding coded bits. The extrinsic mutual information I_E are similarly defined. Both variable and check node reliability messages are approximated with Gaussian messages. Consequently, the *a priori* and extrinsic messages of the SSD block have Gaussian distribution because they represent extrinsic and *a priori* messages for the VND block. Mutual information between corresponding messages and coded bits is therefore determined from the variance of the reliability messages, such as in [4].

It is shown in [4] that by using the EXIT functions (charts) as a visualization tool and by changing the code profile, the error-rate performance can be significantly improved. However, the authors considered only fully random LDPC codes. In this work, the EXIT chart analysis and code design are applied to block-structured irregular LDPC codes while assuming inner soft sphere detection. Rayleigh fading and Winner 3GPP-LTE MIMO channels are considered with four transmit/receive antennas and 16-QAM modula-

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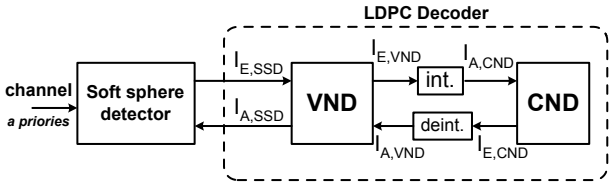


Fig. 1. Tracking of *a priori* and extrinsic mutual information; iterative detection-decoding receiver with inner SSD and outer LDPC decoder.

tion. In order to insure convergence between the inner soft detector and the outer LDPC decoder for a given SNR threshold, the EXIT curve of combined SSD and VND blocks needs to be strictly above the CND EXIT curve, as shown in [4].

The transfer functions of the VND and CND blocks are determined as in [4]. The transfer function of the SSD block is obtained by simulations since there is no closed-form expression. Variances of *a priori* and extrinsic messages are tracked for a large number of channel realizations. It is determined that a second or at most third-order polynomial curve well interpolates the evolution of *a priori* into extrinsic mutual information. Once the EXIT chart of the SSD block is determined, the combined VND-SSD (or extended VND) EXIT chart can be obtained. The combined EXIT chart represents a function of variable-node degree d_V, code rate R and zero error probability E_b/N_0 threshold:

$$I_{E,VND} = f_{VND+SSD}\left(I_{A,VND}, d_V, \frac{E_b}{N_0}, R\right). \qquad (1)$$

The positioning of the VND-SSD EXIT curve strictly above the CND EXIT curve is performed by changing the code profile: different variable and check-node degrees are tested for predetermined code rate and zero error probability threshold. In this work, we seek to improve the detector-decoder performance in lower SNR conditions through the design of modified LDPC codes. Therefore, the chosen zero error probability thresholds for all channel environments correspond to large frame error-rate (close or equal to 1), with the original non-optimized code profile and moderate codeword size (several thousands of bits). The design constraint applied in this work is to preserve the block-structure of PCMs. Therefore, only a reduced set of values for check-node and variable-node degrees is available.

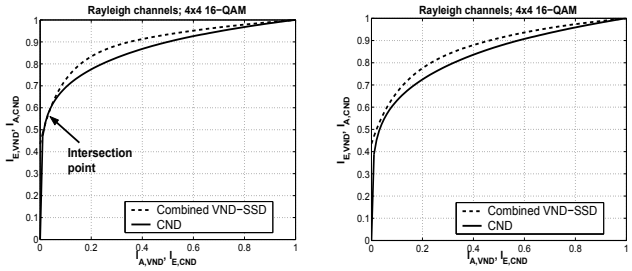
3. DESIGN OF LDPC CODES IN RAYLEIGH FADING CHANNELS

We first present the design of a block-structured LDPC code for Rayleigh frequency non-selective channels. A wireless system with four transmit/receve antennas and 16-QAM modulation is assumed. The original block-structured PCM has 24 block columns and 12 block rows as specified in [3]. All check nodes have degree d_C=8, while variable node degrees are:

$$\begin{aligned} d_{V,1} &= 2,\ v_1 = 12/24;\ d_{V,2} = 3,\ v_2 = 7/24 \\ d_{V,3} &= 9,\ v_3 = 2/24;\ d_{V,4} = 11,\ v_4 = 3/24, \end{aligned} \qquad (2)$$

where v_i is the fraction of variable nodes having degree $d_{V,i}$.

Figure 2(a) shows the EXIT chart of the combined VND-SSD block for the SNR threshold of 8 dB, as well as the CND EXIT chart. The LDPC code profile from Eq. 2 specified for the IEEE 802.11n standard is considered. It can be noticed that there is a region around small values of $I_{A,VND}$ and $I_{E,VND}$ where the combined VND-SSD EXIT curve intersects the CND EXIT curve. This indicates no convergence towards the zero error probability (both *a priori* and extrinsic mutual information are equal to one) for the specified SNR threshold value.



(a) EXIT charts of original LDPC code.

(b) EXIT charts of newly designed LDPC code.

Fig. 2. Combined VND-SSD EXIT curve and CND EXIT curve. Original and newly designed LDPC code profiles, rate = 1/2, inner soft sphere detection, threshold E_b/N_0=8 dB, Rayleigh fading channels, 4x4 16-QAM.

For the predetermined code rate and zero error threshold, the EXIT chart of VND-SSD and CND blocks depends on the variable node degree and check-node degree, respectively. However, if the check-node degree is modified the variable node degree is also modified, and vice-versa. If the average check node degree is decreased, the CND EXIT curve moves further away from the y-axis helping separate it from the VND-SSD EXIT curve. But, at the same time, the variable node degree is also decreased and the VND-SSD EXIT curve is moving down and closer to the CND EXIT curve. The design of the new LDPC code profile has the following steps, and the identical procedure is applied for all channel environments:

1. Choose code rate, zero error-rate threshold, and determine EXIT chart of the SSD block.
2. Decrease check node degree, the resolution step depends on the number of block-columns. Adjust the variable-node degree profile, the resolution step depends on the number of block-rows in the PCM.
3. Repeat previous step until the VND-SSD EXIT chart is strictly above the CND EXIT chart.
4. If it is not possible to find a code profile that insures no intersection between EXIT curves, then increase the zero error-rate threshold and restart the code design process.

The profile of the newly designed LDPC code is shown by Eq. 3 and Eq. 4 which supports the block-structured form of PCM, and the modular LDPC decoder architecture from [3] can be reused. Figure 2(b) shows the combined VND-SSD EXIT curve strictly above the CND EXIT curves, which insures convergence between the inner detector and outer decoder.

$$d_{C,1} = 7,\ \ c_1 = 11/12; d_{C,2} = 8,\ \ c_2 = 1/12, \tag{3}$$

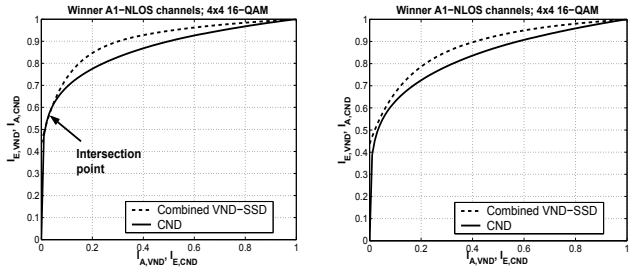
where c_i is the fraction of check nodes having degree $d_{C,i}$,

$$\begin{aligned} d_{V,1} &= 2,\ v_1 = 12/24;\ d_{V,2} = 3,\ v_2 = 8/24 \\ d_{V,3} &= 9,\ v_3 = 3/24;\ d_{V,4} = 10,\ v_4 = 1/24. \end{aligned} \tag{4}$$

4. DESIGN OF LDPC CODES IN 3GPP-LTE WINNER CHANNELS

The design of block-structured LDPC codes for 3GPP-LTE Winner channels [10] is presented in this section. In particular, indoor A1-NLOS and outdoor B1-NLOS (non line of sight) channels [10] are considered with the speed of the mobile user of 5km/h and 70 km/h, respectively.

The EXIT chart of the combined VND-SSD detector for the Winner A1-NLOS channel is shown in Fig. 3(a) together with the CND EXIT curve. The zero-error SNR threshold is 2 dB. The code profile from Eq. 2 is initially considered. Again, the small region where the EXIT chart of the extended VND block intersects the CND EXIT curve can be observed which prevents convergence of the iterative receiver structure. Figure 3(b) shows that the same code profile designed for Rayleigh fading channels (Eq. 3 and Eq. 4) also provides convergence in Winner A1-NLOS channels.



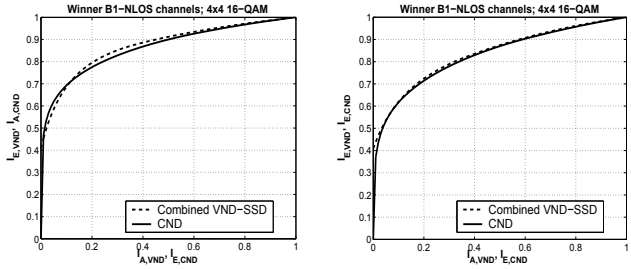
(a) EXIT charts of original LDPC code.

(b) EXIT charts of newly designed LDPC code.

Fig. 3. VND-SSD EXIT curve and CND EXIT curve; original and newly designed LDPC code profiles, rate = 1/2, inner soft sphere detection, threshold E_b/N_0=2 dB, Winner A1-NLOS channels, 4x4 16-QAM.

The EXIT chart of the extended VND block for an SNR threshold of 0.5 dB in Winner B1-NLOS channels is shown in Fig. 4(a) together with the CND EXIT chart for the LDPC code profile given by Eq. 2. It can be clearly noticed that there is an intersection between the two EXIT charts. Consequently, there is no convergence between the inner detector and outer decoder for the particular SNR threshold value.

The LDPC code profile designed for the Winner B1-NLOS channels is given by Eq. 5 and Eq. 6 for check-node and variable-node degree profiles, respectively. The block-structured form of PCM with 12 block-rows and 24 block-columns is still preserved. The average check-node degree is again lower providing a larger



(a) EXIT charts of original LDPC code.

(b) EXIT charts of newly designed LDPC code.

Fig. 4. VND-SSD EXIT curve and CND EXIT curve; original and newly designed LDPC code profiles, rate = 1/2, inner soft sphere detection, threshold E_b/N_0=0.5 dB, Winner B1-NLOS channels, 4x4 16-QAM.

distance from the y axis for the CND EXIT curve.

$$d_{C,1} = 6,\ \ c_1 = 9/12;\ \ d_{C,2} = 7,\ \ c_2 = 3/12, \tag{5}$$

$$\begin{aligned} d_{V,1} &= 2,\ v_1 = 12/24;\ d_{V,2} = 3,\ v_2 = 9/24 \\ d_{V,3} &= 4,\ v_3 = 1/24;\ d_{V,4} = 9,\ v_4 = 1/24 \\ d_{V,5} &= 11,\ v_5 = 1/24. \end{aligned} \tag{6}$$

5. ERROR-RATE PERFORMANCE OF NEWLY DESIGNED LDPC CODES WITH FINITE CODEWORD SIZE

The LDPC code with newly designed profile and infinite (or very large) codeword size achieves zero-error probability for the SNR value greater than or equal to the specified threshold. The convergence speed depends on the relative positions of CND and VND-SSD EXIT functions. However, a large LDPC codeword size is not suitable for efficient decoder implementation. Therefore, we consider the newly designed LDPC code profiles applied on moderate (implementable) codeword sizes, such as hundreds or thousands of information bits. New PCMs are obtained from the original non-optimized matrices by replacing a certain number of non-zero sub-matrices with zero sub-matrices according to the newly designed code profile. At the same time, the number of short cycles (cycles of length 4, 6, and 8) is reduced by choosing the appropriate shift values for the identity sub-matrices. Tables 1 and 2 show the reduction in the number of short cycles after modifying the shift values for two newly designed code profiles which improves system performance.

Figure 5 and Fig. 6 show frame error rate performance in Rayleigh and Winner channels, respectively. The inner soft sphere detector from [1] is considered. The LDPC code size is 1944 bits, the code rate is 1/2, and modified shift values are applied for the newly designed block-structured PCMs with 24 block-columns and 12 block-rows. An error-rate performance improvement of about 1 dB can be observed.

Table 1. Number of short cycles in original and new PCMs; designed code profile for Rayleigh channels.

Cycle-length	Original shift values	New shift values
4	64	12
6	8,242	6,158
8	375K	276K

Table 2. Number of short cycles in original and new PCMs; designed code profile for Winner B1-NLOS channels.

Cycle-length	Original shift values	New shift values
4	81	42
6	8,343	6,245
8	382K	302K

6. CONCLUSION

The design of block-structured LDPC codes is performed for inner soft sphere detection in different channel environments. The EXIT chart analysis is used as a design tool. In order to preserve the block-structure of the parity-check matrices, a reduced set of possible values for check-node and variable-node degrees is available during the design process. The error-rate performance improvement is achieved for a finite codeword length with newly designed code profiles.

7. REFERENCES

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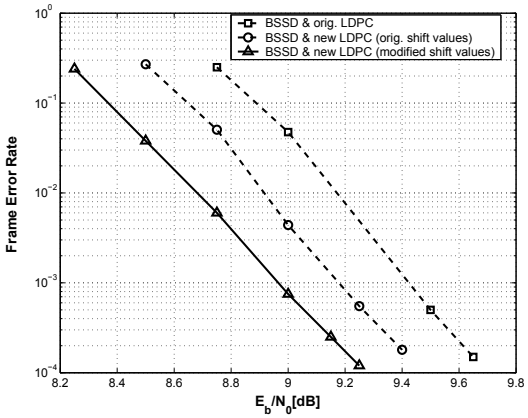

Fig. 5. Frame-error rate performance of bounded SSD with original and newly designed block-structured LDPC codes (old and modified shift values); Rayleigh fading channels, 4x4 16-QAM, 4 outer iterations, 15 inner LDPC iterations.

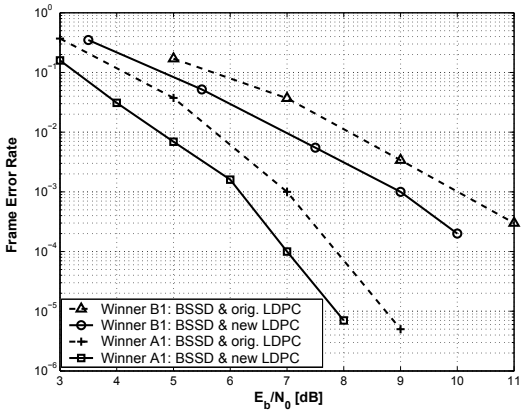

Fig. 6. Frame-error rate performance of bounded SSD with original and newly designed block-structured LDPC codes; Winner A1-NLOS and Winner B1-NLOS channels, 4x4 16-QAM, 4 outer iterations, 15 inner LDPC iterations.