DESIGN OF BS TRANSCEIVER FOR IEEE 802.16E OFDMA MODE

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ABSTRACT

Wordwide Interoperability for Microwave Access (WiMAX), or the IEEE 802.16d/e standard, is a technology for broadband wireless access (BWA) with significant market potential. In this paper, we propose a base station (BS) physical layer (PHY) transceiver solution for WiMAX orthogonal-frequency division-multiplexing access (OFDMA) mode. Our aim is to provide a single chip solution for baseband processing of WiMAX PHY. The data throughput should achieve 20Mbps both for uplink and downlink. The solution is implemented on Cell Broadband Engine, which is a multicore processor jointly developed by IBM, SONY and Toshiba for high performance computing(HPC). Algorithms for symbol timing offset, carrier frequency offset, channel estimation and Space-Frequency Block Code (SFBC) are embedded in this transceiver. Simulation and real test on Cell show that the proposed solution can fulfill the bit-error-rate (BER) requirements under most situations.

Index Terms— WiMAX, OFDMA, MIMO, throughput, Cell Broadband Engine.

1. INTRODUCTION

Broadband wireless access (BWA) has attracted much attention recently. As a BWA solution, Worldwide Interoperability for Microwave Access (WiMAX) is accepted by carriers of worldwide for broadband wireless service. It is estimated that overall broadband market could be 20Billions in 2010 with the mobile WiMAX piece expected to be about 7Billions. WiMAX standard can be classified as Fixed WiMAX (IEEE 802.16d version [1]) and Mobile WiMAX (IEEE 802.16e version [2]). It can be used in hotspot, urban and rural area as an alternative selection for broadband access. Its core techniques, such as OFDMA and MIMO, will be used in next generation wireless/mobile communication system.

At present, there are some chipsets for WiMAX solution, such as Wavesat DM256, Intel 2250 and Picochip PC203 etc.. Most of those chipsets are for 802.16d version, and some of them are designed for customer premises equipment (CPE). Few telecom equipment providers can provide base station (BS) solution for 802.16e with ready chipsets, while 802.16e is more attractive for its mobility support contrasted with 16d. For the WiMAX BS design, customized platform composed of DSP arrays with FPGA acceleration dominates the BS market. Compared with the BS platform based on Open wireless architecture (OWA), they are less flexibility and scalability, especially when multiple standard coexistence and the new services added continuously. Our aim is to provide a single chip solution for 802.16e PHY baseband processing, based on general IT platform with multicore. Processing capability, cost and power consumption are three important factors for system design. Considering these factors, we propose a general design rule for WiMAX BS implementation. That is selecting algorithms for each module of BS with relative light computation load under the system performance requirements. Based on this design rule, we develop a general WiMAX BS architecture (IEEE 802.16e OFDMA-mode) and select the corresponding algorithms for each module. The test on IBM Cell blade server shows that the bit error rate (BER) can achieve the system performance requirements and one Cell processor can support both downlink and uplink of a BS baseband with 20Mbps throughput.

The following paper is organized as follows. The signal model and system architecture is described in section 2. Section 3 introduced the algorithm selection of key components in the system. And the implementation on Cell processor is introduced in section 4. Finally, we conclude the paper in section 5.

2. SIGNAL MODEL AND SYSTEM ARCHITECTURE

In this section, we introduce the uplink signal model of WiMAX OFDMA-mode. The overall block diagram of the proposed BS physical layer baseband transceiver is depicted in Fig.1.

In the downlink shown in Fig.1, after channel coding, modulation, map constellation, ifft and cyclic prefix (CP) insertion, the time-domain samples of an OFDM symbol can be obtained from frequency-domain symbols as

$$x(n) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} X(k) e^{j2\pi nk/N} \quad -N_{CP} \leqslant n \leqslant N-1 \tag{1}$$

where *X(k)* is the modulated data on the *k*th subcarrier of one OFDM symbol, N is the number of subcarriers and N_{CP} is the length of cyclic prefix.

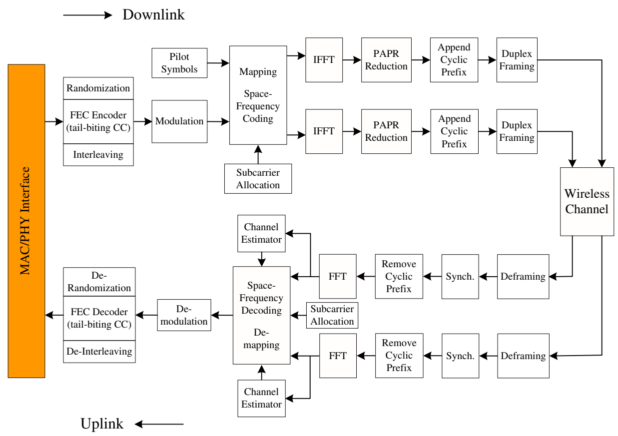

Fig. 1. WiMAX Physical Layer Block Diagram

The impulse response of multi-path channel can be approximately denoted as:

$$h(\tau, t) = \sum_{l=1}^{L} \alpha_l(t)\delta(\tau - \tau_l) \tag{2}$$

where L is the total number of paths, α_l and τ_l are the complex gain and time delay of the lth path. It supposes that the signals are transmitted over a quasi-static multipath fading channel, that is to say, the channel varies much slowly and the fading coefficients can be assumed to be constant during the OFDM block.

Assuming perfect time and frequency synchronization, the model of received signal at the BS after removal of the CP can be written as

$$y(n) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} H(k)X(k)e^{j2\pi nk/N} + z(n) \quad 0 \leqslant n \leqslant N-1 \tag{3}$$

where $H(k)$ is the channel frequency response at the kth subcarrer and $z(n)$ is the additive white complex Gaussian noise (AWCGN).

3. TRANSCEIVER FUNCTION BLOCKS

For the downlink of WiMAX PHY, the algorithm of each module, such as FEC(Forward Error Control) coding, modulation, map constellation, etc., is mature relatively. Thus we focus on the discussion of algorithm selection for uplink block in this paper.

3.1. Synchronization

Timing and frequency synchronization are two important tasks needed to be performed by the receiver. In this paper, ML algorithm based on the CP [3] is chosen to achieve the symbol timing and carrier frequency synchronization. The estimation

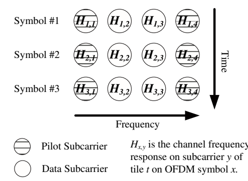

Fig. 2. Pilots and Data Subcarriers for Channel Estimation

of the normalized STO (symbol timing offset)θ and the normalized CFO (carrier frequency offset) ε are derived as (for the derivation in details, please see [3] for reference):

$$\hat{\theta}_{ML} = arg\max_{\theta} \{|\gamma(\theta)| - \phi(\theta)\}. \tag{4}$$

$$\hat{\varepsilon}_{ML} = -\frac{1}{2\pi}\gamma(\hat{\theta}_{ML}). \tag{5}$$

where $\gamma(m)$ is a sum of L consecutive correlations between pairs of samples spaced N samples apart. The term $\phi(m)$ is an energy term, independent of the frequency offset ε.

Once the STO and CFO are estimated, the received time samples can be corrected as follows:

$$y(n)_{corrected} = y(n + \hat{\theta}_{ML})e^{\frac{-j2\pi n\hat{\varepsilon}_{ML}}{N}}. \tag{6}$$

3.2. Channel Estimation

It is well known that it is necessary to remove the amplitude and phase shift caused by the channel.

Based on the uplink tile structure, shown as Fig.2, the pilot-aided channel estimation methods can be employed, which consist of algorithms to estimate the channel at pilot frequencies and to interpolate the channel. The estimation of the channel at the pilot frequencies can be based on least square (LS), minimum mean-square (MMSE) or least mean-square (LMS). Though MMSE has been shown to perform much better than LS, it needs knowledge of the channel statistics and the operating SNR [4]. The interpolation of the channel can depend on linear interpolation, second order interpolation and low-pass interpolation etc.. Considering the tradeoff between feasibility of implementation and system performance, we choose linear interpolation in time and frequency on a tile-by-tile basis for each subchannel.

When the data and pilot information has been assembled as shown in Fig. 2, it is possible to calculate $H_{1,1}$, $H_{1,4}$, $H_{3,1}$ and $H_{3,4}$ using the equation:

$$\hat{H}_p(t, m) = \frac{Y_p(t, m)}{S_p(t, m)} \tag{7}$$

for the mth OFDMA symbol of the tth tile where:

$Y_p(t, m)$ is the pth received pilot subcarrier

$S_p(t, m)$ is the pth transmitted pilot subcarrier.

We omit the index of receive antenna here, since channel estimation for each receive antenna is performed independently.

Subsequently, frequency domain linear interpolation is performed to calculate channel estimates using the following equations:

$$\hat{H}_{1,2}=\frac{1}{3}\cdot(\hat{H}_{1,4}-\hat{H}_{1,1})+\hat{H}_{1,1},\quad \hat{H}_{1,3}=\frac{2}{3}\cdot(\hat{H}_{1,4}-\hat{H}_{1,1})+\hat{H}_{1,1}$$
$$\hat{H}_{3,2}=\frac{1}{3}\cdot(\hat{H}_{3,4}-\hat{H}_{3,1})+\hat{H}_{3,1},\quad \hat{H}_{3,3}=\frac{2}{3}\cdot(\hat{H}_{3,4}-\hat{H}_{3,1})+\hat{H}_{3,1} \quad (8)$$

where $H_{m,k}$ is the channel frequency response at the kth subcarrier of the mth OFDM symbol and $\hat{H}_{m,k}$ is the estimation of $H_{m,k}$.

Finally, time domain linear interpolation is achieved as follows:

$$\hat{H}_{2,1}=\frac{1}{2}\cdot(\hat{H}_{1,1}+\hat{H}_{3,1}),\quad \hat{H}_{2,2}=\frac{1}{2}\cdot(\hat{H}_{1,2}+\hat{H}_{3,2})$$
$$\hat{H}_{2,3}=\frac{1}{2}\cdot(\hat{H}_{1,3}+\hat{H}_{3,3}),\quad \hat{H}_{1,4}=\frac{1}{2}\cdot(\hat{H}_{1,4}+\hat{H}_{3,4}). \quad (9)$$

When all of the channel estimates have been formed, these estimated values are transmitted to the space-frequency decoding module for the data detection using ML method.

3.3. SFBC

A user-supporting transmission using transmit diversity configuration in the uplink, shall use a modified uplink tile. The pilots in each tile shall be split between the two antennas and the data subcarriers shall be encoded in pairs after constellation mapping, as depicted in Fig. 3. Because this is applied in the frequency domain (OFDM carriers) rather than in the time domain (OFDM symbols), we note it as space-frequency block coding (SFBC) [5].

Defined $H^{(i,j)}_{m,k}$ as the channel frequency response at the kth subcarrier of the mth OFDM symbol corresponding to the ith transmit and the jth receive antenna pairs, and $Z^{(j)}_{(m,k)}$ as the frequency response of the AWCGN on the kth subcarrier of the mth OFDM symbol at antenna $j$respectively, on the assumption that the neighboring subcarriers have the same frequency response, the estimation of X_1 and X_2 are:

$$\hat{X}_1=\arg\min_{\hat{X}_1\in\mathbf{X}}\left[\left(\sum_{i=1}^{2}\sum_{j=1}^{2}\left|\hat{H}^{(i,j)}_{1,2(3)}\right|^2-1\right)\left|\hat{X}_1\right|^2+d^2\left(\tilde{X}_1,\hat{X}_1\right)\right]$$
$$\hat{X}_2=\arg\min_{\hat{X}_2\in\mathbf{X}}\left[\left(\sum_{i=1}^{2}\sum_{j=1}^{2}\left|\hat{H}^{(i,j)}_{1,2(3)}\right|^2-1\right)\left|\hat{X}_2\right|^2+d^2\left(\tilde{X}_2,\hat{X}_2\right)\right] \quad (10)$$

where

$$\tilde{X}_1=\sum_{i=1}^{2}\sum_{j=1}^{2}\left|\hat{H}^{(i,j)}_{1,2(3)}\right|^2X_1+\sum_{j=1}^{2}\left(\hat{H}^{(1,j)}_{1,2}\right)^*Z^{(j)}_{1,2}+\sum_{j=1}^{2}\hat{H}^{(2,j)}_{1,3}\left(Z^{(j)}_{1,3}\right)^*$$
$$\tilde{X}_2=\sum_{i=1}^{2}\sum_{j=1}^{2}\left|\hat{H}^{(i,j)}_{1,2(3)}\right|^2X_2-\sum_{j=1}^{2}\hat{H}^{(2,j)}_{1,2}\left(Z^{(j)}_{1,2}\right)^*+\sum_{j=1}^{2}\left(\hat{H}^{(1,j)}_{1,3}\right)^*Z^{(j)}_{1,3} \quad (11)$$

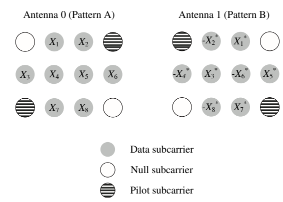

Fig. 3. Pilots and Data Subcarriers in SFBC Mode

Table 1. Parameters for WiMAX OFDMA-mode

Symbol	Description	WiMAX value
B	Bandwidth (MHz)	10
F_s	Sampling frequency (MHz)	11.2
N_{FFT}	No. of subcarriers	1024
G	Guard fraction	1/8
N_{CP}	Guard length	128
Δf	Subcarrier spacing (kHz)	10.94
T_b	Useful symbol time (μs)	91.4
T_g	Guard time (μs)	11.4
T_s	OFDMA symbol time (μs)	102.9

4. IMPLEMENTATION ON CELL BROADBAND ENGINE

Based on the algorithms selected in section 3, we implement the uplink and downlink of WiMAX PHY (baseband) on a single Cell processor, which contains a Power Processing Element (PPE) and eight Synergistic Processing Elements (SPEs) with 256KB on-chip local store, as Fig.4[6]. Table 1 shows the parameters setting of the BS. We use convolutional code as the FEC (constraint length is 7, data rate is 1/2), 16QAM modulation, and $2R_x$x$2T_x$ MIMO technique.

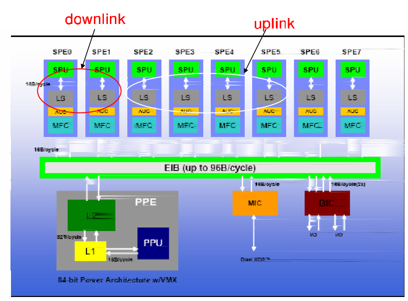

Fig. 4. Workload Partition on Cell Processor (Source: cell diagram from [6])

Our aim is to design a system which can process 20Mbps raw data both for uplink and downlink. Through workload analysis, the bottleneck of system design is the uplink, consisting of synchronization, channel estimation, SFBC and Viterbi decoding. All those modules are computation intensive. In order to integrate all modules of baseband to one chip, we should optimize each module to let it consume as small as computation resource and memory. Considering the powerful floating calculation capability of SPU and its limited local store (256KB), we should tradeoff between the computation performance and memory consumption. The optimization techniques used in our system include: reducing branch, SIMD (single instruction multiple data), pipeline and dual issue. The speed-up rates of components with heavy computation load are shown in Fig.5

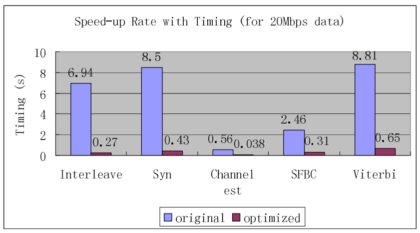

Fig. 5. Speed-up Rates of Key Components

Through careful workload partition, the downlink can be completed in two SPUs and the uplink can be completed in four SPUs, as shown in Fig.4. Figure 6 illustrates the simulation results at different stages of system, such as the signal constellation, the time-domain wave and the power spectral density (PSD). And the bit-error-rate performance obtained from real test on Cell blade server QS20, is shown in Fig.7 for AWGN and Rayleigh channel(SUI-3 model [7]) respectively. The test results certify that the single chip solution we proposed can satisfy the BER requirements. Currently, we are preparing the conformance test for our solution.

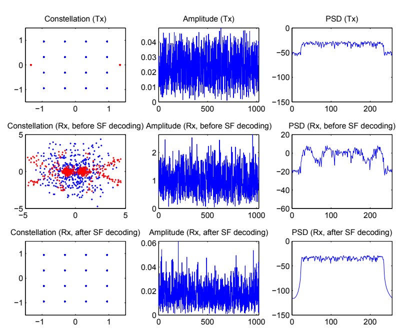

Fig. 6. Simulation Results at Different Stages of the System-level Simulator

5. CONCLUSION

In this paper, we propose a single chip solution for WiMAX PHY broadband processing based on Cell Broadband Engine. The throughput of system can achieve 20Mbps both for uplink and downlink. And the BER performance is satisfied compared with other WiMAX BS system. The preliminary results

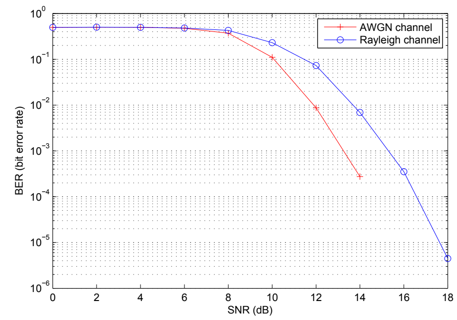

Fig. 7. BER Performance under Different Channel on QS20

we obtained prove that the general IT platform with multi-core has good performance for wireless application. Moreover, high performance general IT platform is a good platform candidate for open wireless architecture. At present, the conformance test of our system with 802.16e is under preparation.

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