ANALOG TO FEATURE CONVERSION

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ABSTRACT

The analog to digital conversion of signals constrains their processing due to the limitation of bandwidth, power and size required for the wide band signals being processed in emerging wireless standards. The solution proposed in this paper is a specially constructed analog processing block ahead of the traditional ADC within a typical RF front-end involving an antenna, filter, LNA, and AGC. This analog block includes a structured matrix of tuneable analog delay elements together with analog summers and attenuators. The analog block can be programmed on-the-fly to form spectral estimates, narrow band filters, correlation detectors, and more. Finally, we show some improved results from the design of FIR filters for these structures.

Index Terms— Mixed analog-digital integrated circuits, Delay circuits, Tunable circuits and devices, Fourier transforms, Filters

1. INTRODUCTION

The analog to digital conversion of signals constrains their processing due to the limitation of bandwidth, power and size required for the wide band signals being processed, especially in the 3-10GHz range. As more of the RF spectrum becomes allocated for communications, and as communications signals cover wider frequency bands, there are increasing performance requirements placed on the ADC and the associated backend processing system, especially for those systems that are general purpose. The present paper describes a method for processing RF microwave signals using a programmable analog processing block (called an analog to feature converter) ahead of the typical analog to digital converter (ADC). This approach can address some of these higher performance requirements by offloading processing ahead of the ADC. The next section covers some of these factors in more detail.

2. ADC AND SIGNAL PROCESSING PERFORMANCE

The primary factors that limit ADC performance are aperture jitter and comparator ambiguity. Aperture jitter in the sample and hold circuit is caused by noisy clocks, temperature drift and other instabilities. Comparator ambiguity results from the necessity of having each comparator determine, after the hold-time period, whether the result is a 0 or a 1. There is a certain probability that at least one comparator will be indecisive. Aperture jitter and comparator ambiguity have contributed to a decrease in the rate of performance improvement of ADCs in recent years.

Coupled to this slowing advance is the backend digital processing system after the ADC. Here the processing performance is driven by the performance of embedded CPUs and memories under Moore's Law, which predicts that CPU performance will double approximately every 18 months. While this theory has held true for many years, recent studies have shown a downward trend in CPU performance advances as well. One study showed performance grew by 58% per year between 1985 and 1996, but slowed to 41% per year recently. These slowing performance numbers are attributed to three effects: total dissipated power, wire delay and memory bottlenecks.

Despite the slowing performance improvements, signal bandwidth continues to increase. Commercial Ultra Wide-Band (UWB) systems based on IEEE 802.15 already use 500MHz of RF bandwidth. CPU performance must also increase correspondingly with the wider bandwidth. One solution to this dilemma would be a fully programmable front-end system-on-a-chip that can both alleviate the ADC requirements as well as back-end digital signal processing.

3. "PASSIVE" TUNABLE RF TECHNOLOGY

Signal processing ahead of the ADC typically has involved custom circuits such as fixed filters, mixers, amplifiers and beamformers which compute simple arithmetic operations on the RF signal. And when more complicated functions are introduced, they have often involved active amplifying devices (such as mixers) which increase signal noise and distortion. Many techniques also are inherently narrowband in nature. But materials, thin-film fabrication and MEMS technology has advanced in recent years so that much more complicated, broadband "passive" front-end processing is becoming possible. Summing properly delayed and attenuated analog signals simply involves bringing them together; MEMS switches can do this with very low loss. Variable attenuation can be implemented with switched networks of resistive materials. Tunable RF time delay has been more challenging, but can be

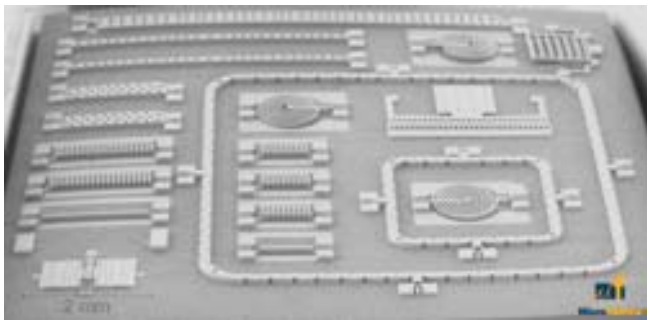

Fig. 1. Microfabrica MEMS Test Structures.

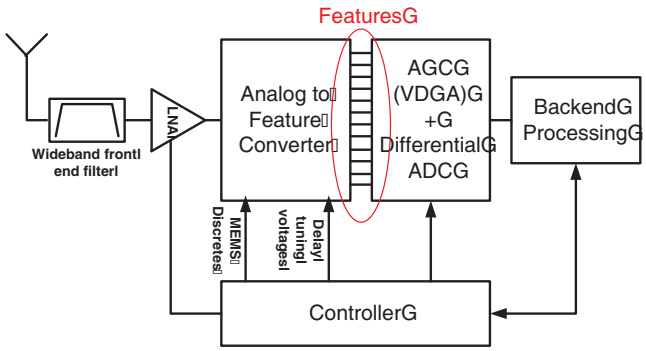

Fig. 2. System Diagram.

implemented by (see Table 1):

- varying the distance RF signals travel
  - MEMS transmission lines with switches (see Figure 1 for Microfabrica test circuits similar to that characterized at Boeing.)
- varying the speed RF signals travel
  - non-linear transmission lines (CMOS/SiGe/GaAs) (see [1]). This typically involves active elements however.
  - changing permittivity - ferroelectric substrate (BST on sapphire)
  - changing permiability - ferromagnetic substrate (YIG ferrite) (see [2] and [3]) Thin film magnetics hold the key to making this technology feasible.

In what follows, we will assume a passive analog to feature conversion technology combining MEMS transmission delay lines (for fixed delays) and ferroelectric delay lines (for tunable delays) together with settable matching resistors and MEMS switches for control of signal summation. This combination provides the best of both MEMS and ferroelectric technologies on a single BST-on-sapphire substrate with no active elements. Active elements could both preceed and follow. Typically a broadband LNA connected to an antenna or other signal source would preceed and another amplifier (typically a VDGA for example) would follow before the ADC to set the final signal level before digitization. A system diagram would look similar to Figure 2.

4. ANALOG TO FEATURE CONVERSION

Figure 3 shows a diagram of the Analog to Feature converter (AtoF). Variable delays can be build out of fixed MEMS transmission line delays (which have low loss) together with short ferroelectric variable delay lines, all on a common substrate. This gives delays on the order of 100's of ps. For longer delays up to 100's of ns, the ferromagnetic approach would be

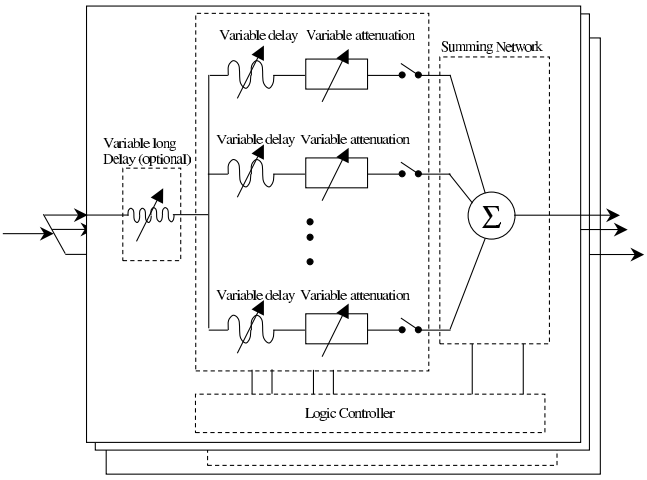

Fig. 3. Analog to Feature integrated chip.

necessary and would involve a separate substrate and material. This analog to feature converter would be able to handle many different applications, such as:

Interference cancellation. The idea is simply to add a signal to itself delayed 180^o out of phase. This provides a very simple notch filter in advance of the ADC. The benefits are critically important in many applications where a small signal of interest (SOI) is masked by a very large signal which would ordinarily fill up the dynamic range of the ADC.

Direct phase demodulation. The SOI could be passed through a bandpass filter implemented in the AtoF converter and then the center frequency could be "correlated" using the same idea as in the AFT where separate sines and cosines of the correct frequency produce essentially the (I,Q) demodulated value of the signal. The ADC would only need to sample at the symbol rate. A separate digitally computed symbol phase could then be fed back into the controller to move the delay values a slight amount in order to track the symbol values. The final digital part of the receiver is almost trivial.

True Time Delay Beamforming. If more than one antenna are input to the AtoF converter, each antenna can be sepa-

Type	Control signal	Area/ps delay	Loss/ps delay	Voltage	Notes
MEMS transmission line delay	Discrete switched	0.05 mm^2	0.006 db	10-20V	Low loss
Non-linear transmission line delay	Discrete switched	0.02 mm^2	Amplified	3.3V	Amplified
Ferroelectric delay (BST)	Continuous voltage	0.09 mm^2	0.04 db	$\pm 20V$	Tuneable
Ferromagnetic delay (YIG)	External magnet	1in^2	0.00002 db	NA	Discrete device
MEMS switch	Discrete voltage	≈ 0.01mm^2	0.1 db loss	10-20V	Fabbed on BST

Table 1. Delay and switch technologies

rately delayed in a controlled fashion to form one or more beams to be fed into the ADC. This allows a much better result in the case of broadband signals than if just phase shifters were used. Due to the architecture that uses a combination of MEMS switches for signal path setup, but continuous voltage lines to tune the ferroelectric delay lines, the reliability of MEMS switches when used in a tracking antenna are not an issue.

Frequency Tracker. When the LO of a transmitter drifts, the transmitted signal changes frequency slightly. A receiver must track this to keep locked on to the center frequency. The ability to tune the delays in a continuous fashion by the AtoF converter means that three slightly offset "tone correlations" can be done at three very close frequencies $\{f_{LO}, f_C, f_{HI}\}$. These three features could be digitized and a simple interpolation done (based on power) to keep the center frequency f_C locked onto the signal.

5. (NT,+,*) TO (+,T) SIGNAL PROCESSING

Basic linear digital signal processing (i.e. Fourier transforms, filters, scaling, matrix and vector operations, etc.) uses three operations on the signal: uniform samples, sums and scalar products. Analog processing can also do these operations, but factors such as dynamic range limitations (especially when doing signal products), component variation and temperature have always limited its use. If we replace uniform sampling with programmable delays and allow an implied scaling before digitization, then the basic linear signal processing operations can be transformed into delays and sums. Two important examples are the Arithmetic Fourier Transform (AFT) and FIR filters.

5.1. Arithmetic Fourier Transform

Besides the usual discrete and fast algorithms, the Fourier transform can also be implemented using the arithmetic Fourier transform (see [4] and [5]). In the algorithm, the N sine and cosine (a_n and b_n) coefficients of a signal of period T are computed using only delays, additions and subtractions of a bandlimited signal $A(t)$, with Fourier series:

$$A(t) = a_0 + \sum_{n=1}^{N} (a_n \cos(2\pi nt/T) + b_n \sin(2\pi nt/T))$$

Define $B(2n, \alpha)$ to be the $2n^{th}$ Bruns alternating average:

$$B(2n, \alpha) = \frac{1}{2n} \sum_{m=0}^{2n-1} (-1)^m A(\frac{m}{2n}T + \alpha T)$$

Then the Fourier coefficients a_n and b_n, of the Fourier series of $A(t)$ can be computed by:

$$a_n = \sum_{l=1,3,5,\ldots}^{[N/n]} \mu(l) B(2nl, 0)$$

$$b_n = \sum_{l=1,3,5,\ldots}^{[N/n]} \mu(l)(-1)^{(l-1)/2} B(2nl, 1/4nl)$$

In this equation, $\mu(t)$ is the Moebius function on the natural numbers which has values $\mu(1) = 1$, $\mu(p^2 k) = 0$ for prime p and integer k and $\mu(p_1 p_2 p_3 ... p_r) = (-1)^r$ for r distinct primes $\{p_i\}$. The positive and negative terms in the sums coming from the Moebius function and sign changes can be separated so that the calculation can be performed by the AtoF converter. The separated terms may then be processed in analog circuitry using delays and sums, and the processed analog terms can then be digitized using a differential ADC directly before sampling. The constant $1/(2nj)$ that is shown as a division can be absorbed into the final sampling process as well, since the feature signals would typically be amplified using a variable digital gain amplifier (VDGA) before sampling by the ADC.

Calculating all N Fourier coefficients requires $O(N^2)$ different signal sample (i.e. phases) instead of the usual N (see [6]). This fact led to research using linear interpolation to cut down the number of "samples" required because the desire was to see if the AFT could be efficiently realized in digital applications. While typical uses of the AtoF converter would only select a subset of the frequencies, it is still important to use as few different delays as possible. This can be done through the use of shared delays, shown conceptually in the figure below. This capability must be built into the AtoF converter when designed.

5.2. FIR Filters

Any type of linear FIR filter can also be implemented using delay and sum operations because arbitrary linear filter re-

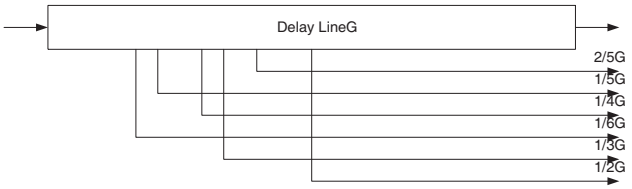

Fig. 4. Shared Farey fraction delays

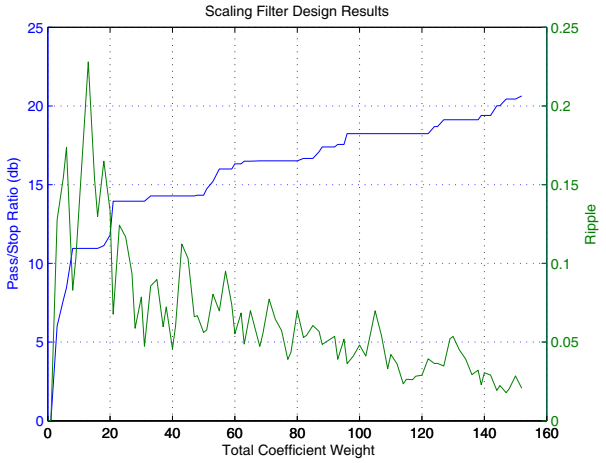

Fig. 5. Scaling Design Method Results

sponses can be approximated by FIR filters using only integer coefficients. The scaling method is a very simple way (without applying discrete optimization techniques) to reduce the number of phase delays and summations necessary to implement a filter using only integer coefficients. The method works as follows. The designed coefficients from a floating point filter are scaled and rounded to integers and the scaling is swept over a wide range from 1 to a large value. The best passband/stopband ratio is recorded until a better one is encountered. As the scaling goes up, so does the total coefficient weight (sum of the absolute values of the integer coefficients) and therefore so does the implementation cost. The results of applying this method to a 31 tap low pass FIR filter with [0 0.1] pass band and [0.2 0.5] stop band (Matlab notation) are shown in Figure 5.

To improve this result requires modifying when a sample is taken (i.e. controlling the phase delay). This can be done using a constrained Monte-Carlo method where scaled versions of a highly oversampled version of the basic filter kernel are "downsampled" by searching in kernel sample space for a set of subsamples that have an approximate difference between them, but vary enough so that the final frequency response can be improved. This method was implemented and the results are shown in Figure 6. Clearly there is often a 2-3db improvement possible in passband to stopband ratio just by choosing non-uniform delays.

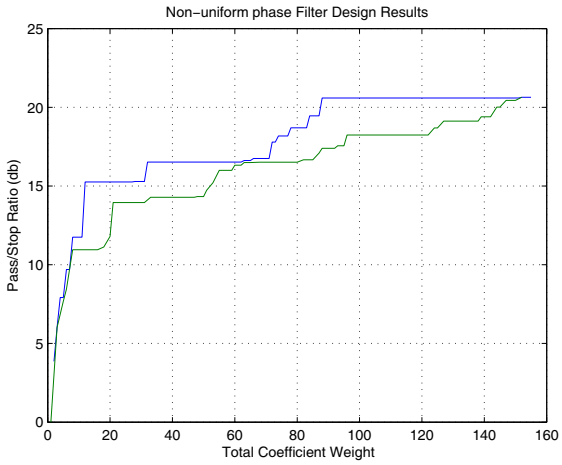

Fig. 6. Non-uniform Phase Monte-Carlo Method

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