EFFICIENT SAMPLE RATE CONVERSION FOR MULTI-STANDARD SOFTWARE DEFINED RADIOS

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ABSTRACT

This paper presents a modified structure based on Cascaded Integrator Comb (CIC) filters and polynomial interpolation to perform arbitrary sample rate alterations. Incorporating CIC compensation filter within the polynomial interpolator has obviated programmable filter typically used in the process. It has also been shown that a maximum passband ripple of 0.5dB is attainable with comparatively fewer computations. The ensuing design leads to an efficient realization both in terms of computational complexity and hardware utilization. This architecture is especially useful in the digital IF stage of emerging multi-standard wireless transceivers where fractional sample rate conversion with large relatively prime factors is required. Proposed solution has been tested by implementing it in a software radio simulation model supporting three commercial wireless communication standards, namely GSM, IS-95 and UMTS.

Index Terms— CIC Compensation Filter, Farrow interpolator, software defined radio, sample rate conversion.

1. INTRODUCTION

Sample rate conversion (SRC) in multi-standard, all digital communication receivers has been a focus of recent research [1-3]. The objective of this process is to efficiently convert signals received from antenna, digitized at ADC sampling frequency, to a data rate that can be conveniently processed by existing DSP processors. Different SRC solutions have been proposed to date of which designs based on Cascaded Integrator Comb (CIC) filters and polynomial interpolation filters are considered suitable for integer and fractional sample rate changes respectively [3]. Some drawbacks have however been noted in these approaches that include poor passband response of CIC filters in wideband signals and long impulse response of polynomial interpolator. Software radio systems developed using these SRC stages hence require high computational and hardware complexity creating implementation bottleneck.



Figure 1: Architecture for arbitrary SRC in Software Radio Systems

A recently proposed SRC architecture for software radio applications, by Yeung and Chang [4], is shown in figure 1. In this approach, a high effort is required for various optimizations at different stages of design that can be a drawback for software radio systems supporting multiple standards. The crux of designing SRC filtering stage is to perform the operations with least computational complexity while satisfying the limits for passband distortion and stopband attenuation. However, to achieve low passband ripple with high stopband attenuation, stringent filter design requirements lead to SRC solutions that are impractical for real time DSP implementation. Specifically, CIC filters have large number of stages while Farrow interpolators have long impulse response that increases the complexity of both solutions. In this paper, a new SRC filter design technique has been proposed that is based on integration of CIC compensation within polynomial interpolation. Flat passband characteristics in the frequency response of ideal Farrow interpolator have been replaced by a second order polynomial that acts as a compensator for the CIC filters. The proposed joint design enhances the power efficiency of the SRC solution while yielding a computationally efficient realization. The rest of the paper is organized as follows: Section 2 presents the modifications made to the architecture of figure 1 to remove the programmable filter stage. Section 3 explains the design of SRC filters and method by which CIC filters and polynomial interpolation have been combined, while the application of proposed SRC scheme on commercial wireless communication standards is included in section 4. Complexity analysis and comparison is presented in section 5.



Figure 2: Proposed Sample Rate Conversion Architecture

2. MODIFIED SRC FILTER

In this section, a modified SRC architecture has been proposed that features CIC compensation embedded within the polynomial interpolation. The block diagram of this system is shown in figure 2. In this structure, maximum possible decimation has been performed in CIC filters since the complexity in each section of a multi-stage architecture is directly proportional to the effective sampling rate of that stage. Numerically, if the number of operations performed in i^{th} stage is N_i and D_i is the product of decimation factors till i^{th} stage, S is the total number of stages, then with F_s being the sampling frequency of ADC, overall complexity 'C' of a multi-stage realization can be expressed as follows [7]:

$$C = \sum_{i=1}^{S} \frac{N_i \times F_s}{\prod_{k=1}^{i} D_k}$$
(1)

Thus a larger value of the denominator ensures that fewer computations are performed per unit time. The structure of figure 2 assumes that the arbitrary rational SRC factor has been factored in the form:

$$\frac{p}{q} = M \times \mu \times 2^k \tag{2}$$

This factorization expresses the SRC ratios into an arbitrary integer part M, a fractional part $\mu \in [1,2)$ and a power of two integer 2^k . Moreover, M for each standard is selected such that large values of M are a product of smaller values corresponding to other standards. This results in a series of multiplexed CIC filters performing integer factor SRC as shown in figure 2. Table 1 lists such factorization for various wireless communications standards with input ADC sampling rate of 80 MSPS.

One important aspect of the proposed system in figure 2 is that the Farrow interpolator operates at a lower sampling rate but not at the lowest possible sampling rate. This leads to relaxed design constraints for the polynomial filter. Consequently, fewer Farrow coefficients are needed with shorter impulse response for the polynomial filter. Thus additional savings in computational complexity have been realized here.

TABLE 1FACTORIZATION OF SRC RATIOS

Standard	Data	SRC	Band-	М	μ	k
	Rate	ratios	Width			
	270.8	677	200	256	1.733	1
GSM	Kbps	200000	KHz			
	1.2288	48	1.25	64	1.966	1
IS-95	Mbps	3125	MHz			
	3.84	6	5	16	1.54	1
UMTS	Mbps	125	MHz			
	48.6	243	30	896	1.08	1
D-AMPS	Kbps	400000	KHz			
IEEE	11	11	22	2	1.1	2
802.11b	Mbps	80	MHz			

3. DESIGN OF COMPOSITE SRC FILTERS

This section explains the design procedure to obtain coefficients of joint Farrow interpolator and CIC compensator block in the modified structure of section 2. The parameters that need to be determined include number of CIC stages, coefficients of Farrow structure and the order of interpolating polynomial. The number of CIC stages has been determined using the out-of-channel attenuation requirements. The design of joint CIC compensation and polynomial interpolation filter has been achieved by defining the desired frequency response of Farrow interpolator as follows:

$$D(\omega) = \begin{cases} 1+K_{p}\omega(\omega_{c}-\omega) & 0 \le \omega \le \omega_{c} \\ 1-\frac{(\omega-\omega_{c})}{\omega_{s}-\omega_{c}} & \omega_{c} \le \omega \le \omega_{s} \\ 0 & \omega \ge \omega_{s} \end{cases}$$
(3)

where ω_c = stopband frequency of CIC filters, ω_s = stopband frequency of Farrow interpolator, and

$$K_p = \frac{4 \times (\max D(\omega) - 1)}{\omega_c^2}$$
(4)

The constant K_p controls the maxima of the second order polynomial. The desired function in equation (3) has been defined as a second order polynomial in the passband, a linear function for the transition band and zero in the stopband. The passband part acts as the compensator for CIC filter droop while the stopband limits ensures sufficient anti-imaging properties for the polynomial filter. Using this desired function, the Farrow interpolator has been designed through minimax optimization scheme using the following frequency domain design equations [6].

$$H(j\omega F_s) = \frac{e^{-j\omega N_2}}{F_s} \sum_{l=0}^{L} C_l(\omega) W_l(\omega)$$
(5)

Where $C_l(\omega)$ corresponds to individual branch filters' frequency response and $W_l(\omega)$ is a weighting function as depicted below [6].

$$C_{l}(\omega) = \begin{cases} \frac{N}{2} \sum_{n=0}^{N-1} c_{l}(n) \cos((\frac{N-1}{2}-n)\omega), \ l \ even \ (6) \\ \frac{N}{2} \sum_{n=0}^{N-1} c_{l}(n) \sin((\frac{N-1}{2}-n)\omega), \ l \ odd \\ W_{l}(\omega) = \begin{cases} \sum_{k=0}^{l} k! \binom{k}{l} \frac{\sin(\omega/2+k\pi/2)}{(\omega/2)^{k+1}}, \ l \ even \\ \sum_{k=0}^{l} k! \binom{k}{l} \frac{\cos(\omega/2+k\pi/2)}{-(\omega/2)^{k+1}}, \ l \ odd \end{cases}$$
(7)

For different values of N and l, the objective is to find the coefficients of Farrow interpolator as close as possible to the desired response given in equation (3). The presence of a preceding CIC filter helps to reduce the order (L) of polynomial and the number of taps (N) in Farrow interpolator impulse response, given that the demand of stopband attenuation is already relaxed by the CIC filter. Since low computational complexity is a priority for proposed SRC solution, only second and third order polynomials have been considered for Farrow interpolator.

4. APPLICATION OF PROPOSED SCHEME

The application of proposed SRC structure has been explained in this section, taking UMTS standard as an example. Basic specifications for UMTS have been provided in table 1. Additionally, UMTS uses QPSK modulation and raised cosine pulse shape filtering with a roll-off factor of 0.22 which makes the passband bandwidth of $0.03F_{in}$ where F_{in} is the sampling rate at transmitter set at 20 times the UMTS symbol rate.

At the receiver end, it is assumed that the signal has all adjacent channels attenuated to a sufficient level. No noise or channel impairments have been considered here since the performance of SRC filters alone is being discussed. The received signal is digitized at an ADC sampling frequency F_s completely independent of the transmitter/symbol rate. In our set-up, F_s is fixed at 80 megasamples per seconds for all standards. After sampling, the signal comprising single channel bandwidth of UMTS is decimated by a factor of M using CIC filters. Employing notations of previous section, and normalizing F_s to 2π , we have the following specifications for the desired frequency response of Farrow interpolator; $\omega_c = 0.0586\pi$ and $\omega_p = 0.117\pi$. Using these

parameters, K_p comes out to be 0.25 using equation (4). As noted in Table 1, a single (k=1) halfband filter is needed to complete the SRC architecture for UMTS. The details of computational costs, passband ripple and stopband attenuation for different configurations of Farrow interpolator in proposed SRC structure are listed in Table 2. The interpolation polynomial has been restricted to a maximum of third order to get the lowest possible computational load. Remaining configuration stays fixed with 4 stages of CIC filters and a halfband filter of 11 taps as these have negligible effect on multiplications per second.

 TABLE 2

 PERFORMANCE OF PROPOSED SRC SOLUTION FOR

 UMTS STANDARD

L	Taps	Passband	Stopband	Computational				
		ripple (dB)	attenuation	Complexity				
			(dB)	(MMPS)				
	2	0.9	-56	124				
2	4	1	-59	154				
	8	0.5	-60	214				
	2	0.9	-56	139.5				
3	4	1.5	-57	179				
	8	2.5	-63	259.5				

5. SIMULATION RESULTS

The proposed SRC structure has been simulated in a software defined radio testbed developed in Matlab. A single channel of IS-95 or UMTS standard has been simulated and subjected to sample rate change from ADC rate to standard specific symbol rate. These standards are similar in the sense that both IS-95 and UMTS use same pulse shaped filter and almost same modulation scheme but with different symbol rates and bandwidth requirements. Simulation results for GSM can be derived in a similar manner.

Figure 4 (inset- above) shows the spectrum of input signal corresponding to UMTS standard after passing through CIC decimator. The horizontal frequency axis in this figure ranges from 0 to $F_s/2$. Although we have assumed a signal free of adjacent channel interference, this figure shows that CIC filter can attenuate adjacent channels up to 75dB. Farrow interpolator (L=2, N=8) response to CIC decimated signal is superimposed on the same diagram. Optimization for combined CIC compensator and Farrow interpolator has been carried out using minimax function of Matlab. Figure 4 (inset- below) shows the response of composite SRC filter i.e. a combined response of CIC decimator, Farrow interpolator and a halfband filter (dotted), while the solid line indicates the desired response that corresponds to spectra of pulse shaped signal before SRC. Similarly, figure 5 shows the input signal spectrum and SRC response for IS-



Figure 4: (a) Frequency Response of **UMTS** Signal after CIC Decimation and Farrow Interpolation. (b) Composite SRC Filter Response.

95 standard. The IS-95 channel occupies lesser bandwidth in comparison with UMTS channel so two multiplexed CIC filters decimate the IS-95 received signal followed by a Farrow Interpolator of third order (L=2, N=8). The SRC stage for IS-95 ends with a single (k=1) halfband filter. As noted in Table 2, a negligible passband distortion exists in all configurations of Farrow Interpolator. However, the proposed structure outperforms existing SRC designs with respect to computational complexity. Specifically, time varying CIC filters require 160 Million multiplications per second while generalized Farrow solution can consume up to 400 Million multiplications per second [3]. Similarly, the DSP based solution presented by Yeung and Chan requires upto 1700 Million multiplications per second [4]. The SRC architecture developed in this work compares favorably with time-varying CIC filtering, as it requires only 200 Million multiplications per second for the UMTS standard. Moreover, the proposed scheme has also been applied to IS-95 and GSM with even fewer computations for the latter standards.

6. CONCLUSION

A low complexity SRC structure has been developed, comprising multiplexed CIC filters, Farrow interpolators and halfband filters. By integrating CIC compensation within the polynomial interpolation, a computationally efficient realization has been derived. The design process is simple and involves obtaining coefficients of Farrow interpolator through minimax optimization. It has been shown that by allowing a small passband ripple of 0.5dB, the low order polynomial filtering and CIC filters result in an SRC architecture that can be efficiently implemented on



Figure 5: (a) Frequency Response of **IS-95** Signal after CIC Decimation and Farrow Interpolation. (b) Composite SRC Filter Response.

a programmable DPS or ASIC platform. The SRC architecture has been tested by simulation in software radio system supporting multiple wireless communication standards.

7. ACKNOWLEDGEMENT

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