EFFICIENT QRD FOR SRI-RLS BASED EQUALIZATION ON PROGRAMMABLE ARCHITECTURE

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***Abstract*- Advanced adaptive filters have been shown to be very powerful for tracking time varying channels in various wireless communications system. However, the performance comes at the expense of highly resource-demanding implementations, especially in the context of programmable architecture based SDR. We present the optimizations for programmable implementation of QRD based SRI-RLS, which represents a large family of advanced adaptive filters. The key contribution of our work is to comprehensively and systematically remove the redundant operations in the QRD for SRI-RLS. Although most signal processing and scientific libraries implement Householder Reflection based QRD, we explore different alternatives and then choose Given Rotations based QRD to enable the aforementioned systematic redundancy removals. Our work significantly reduces the resource requirements (cycle count, energy consumption, etc.) of SRI-RLS implementation. Comparing to the widely accepted QRD implementation in Numerical Recipes, our work reduces 96.4% cycle-count on a typical baseband DSP (TI TMS320C6713), enabling efficient implementations. The paper shows that removing redundancy is very effective for modern statistical signal processing algorithms that largely rely on cascaded matrix operations.**

Keywords: **Equalizer, QRD, DSP Implementation, Software Defined Radio**

I. INTRODUCTION

Signal processing complexity in wireless communication increases exponentially with the increment of spectrum efficiency [1]. Hence, although the Moore's law made a fairly optimistic prediction for the evolution of semiconductor industry, increased silicon capability is easily exhausted by the explosion of signal processing complexity in wireless communication. This brings a very challenging gap to bridge. In the context of Software Defined Radio (SDR), the gap becomes even more challenging, because the flexibility of programmable architecture comes at the expense of lower efficiency and reduced energy efficiency. In order to bridge the gap, we need to have scalable implementation that enable the system to finely adapt to operation conditions and user requirements, resulting in higher efficiency [2][15].

Targeting high performance and efficient equalization on programmable architectures, our work is to optimize the Square-Root-Information Recursive-Least-Square (SRI-RLS), a powerful updating algorithm representing a large class of advanced adaptive filters utilizing square root information, orthogonal transformation or projection principles [3]. In fact, similar algorithms are often intensively applied to tackle space-time channel and multiple-dimensional signals in emerging wireless transmission schemes such as OFDM-MIMO [4]. Comparing to other popular adaptive filter algorithms such as Least Mean Square (LMS) and variants, SRI-RLS exhibit superior convergence performance and noise immunity, so that it significantly outperform LMS style algorithms in HSDPA chip equalization for harsh channels such as 3GPP case 3 [5] and ITU Veh.A [6].

However, the performance gain of SRI-RLS comes at the cost of much higher complexity. The orthogonal triangular decomposition (QRD), core of SRI-RLS, has the complexity being $\Theta(N^3)$, whereas LMS has only linear complexity. Hence the implementation of SRI-RLS should be carefully optimized.

The realization of QRD has been studied for decades. On the hardware side, there are many papers on the CORDIC based QRD. Usually, the QRD fabric consists of a triangular array of CORDIC units [7]. On the software side, the high performance computing community and radar signal processing community have been investigating effort for long time. Both real and complex QRD are present in LAPACK and similar libraries (ScaLAPACK, LINPACK, etc.) [8]. A similar implementation is introduced in Numerical Recipes [9], where algorithm, data layout and memory access are all intensively optimized by hand.

The key contribution of our work is *comprehensive and systematic redundancy removal*. Since many modern statistical signal processing algorithms rely on cascaded matrix operations, the direct implementation of mathematical formulations has lots of redundancy inside. In order to support the redundancy removal in SRI-RLS, we implement QRD based on Given Rotations (GR) instead of Householder Reflection (HR), which is implemented in most scientific and signal processing libraries [8][9].

The remaining part of the paper consists of the following sections: Section II briefs the SRI-RLS based equalization; Section III introduces the algorithm alternatives; Section IV presents the details of redundancy removal; Section V concludes the paper and briefs future work.

II. QRD BASED SRI-RLS FOR HSDPA EQUALIZATION

The equalization is performed with a complex-tap FIR filter, and the coefficients of the FIR filter are adapted based on the

error between the equalizer output and the known pilot (reference signal) based on the Mean Square Error criterion. For chip level equalization in Code Division Multiple Access systems, this is

$$\mathbf{g}_{a_j}^j = \arg\min_{\mathbf{g}_{a_j}^j} \mathrm{E}(\| \mathbf{g}_{a_j}^j \mathbf{Y}_{a_j} \mathbf{C}_p^{j\,\mathrm{H}} - \mathrm{s}_p^j \|^2), \quad (1)$$

where $\mathbf{g}_{a_j}^j$ is the complex weighting vector to optimize, $\mathbf{Y}_{a_j}$ is the received data associated with the pilot, and $\mathbf{C}_p^{j\,\mathrm{H}}$ is the pilot code matrix of the j th base-station, s_p^j transmitted pilot symbol which is known by receiver in prior, where $\| \bullet \|$ is the norm of a complex vector. More details of the model can be found in [10].

QRD based SRI-RLS is a very powerful adaptive filter algorithm. It shares the fundamental principles with many other advanced adaptive filters [3]. The key of QRD-RLS is the QRD based updating step:

$$\begin{bmatrix} \mathbf{R}'^j_{a_j}[i] & \mathbf{z}^j_{a_j}[i] \\ \mathbf{0} & \bullet \end{bmatrix} \leftarrow \mathbf{T}_p^j[i] \times \begin{bmatrix} \lambda \mathbf{R}'^j_{a_j}[i-1] & \lambda \mathbf{z}^j_{a_j}[i-1] \\ \mathbf{Y}_{a_j}[i-1]\mathbf{C}_p^j[i]^{\mathrm{H}} & s_p^j[i] \end{bmatrix}, \quad (2)$$

where λ is the forget factor determined by channel coherence time, $\mathbf{R}'^j_{a_j}[i-1]$ is a upper triangular matrix at time instance i and $\mathbf{z}^j_{a_j}$ is the corresponding right hand side, $\mathbf{T}_p^j[i]$ represents the orthogonal updating matrix at the i -th symbol instant and it is the transpose of $\mathbf{Q}$, which is the result of QRD.

The QRD is defined as:

$$\mathbf{A} = \mathbf{QR}, \quad (3)$$

which means that the original matrix $\mathbf{A}$ is decomposed into two matrixes: the upper triangular matrix $\mathbf{R}$ and the orthogonal matrix $\mathbf{Q}$. Since $\mathbf{Q}$ is orthogonal, $\mathbf{Q}^\tau \mathbf{Q} = \mathbf{I} \Leftrightarrow \mathbf{Q}^\tau = \mathbf{Q}^{-1}$. Hence we get

$$\mathbf{R} = \mathbf{Q}^{-1}\mathbf{A} = \mathbf{Q}^\tau \mathbf{A} \quad (4)$$

Define

$$\mathbf{A} = \begin{bmatrix} \lambda \mathbf{R}'^j_{a_j}[i-1] & \lambda \mathbf{z}^j_{a_j}[i-1] \\ \mathbf{Y}_{a_j}[i-1]\mathbf{C}_p^j[i]^{\mathrm{H}} & s_p^j[i] \end{bmatrix}, \quad (5)$$

After getting $\mathbf{R}'^j_{a_j}[i]$ and $\mathbf{z}^j_{a_j}[i]$ based on Eq.(2), the $\mathbf{g}^j_{a_j}$ in Eq.(1) can be derived with simple back substitution:

$$\mathbf{R}^j_{a_j}[i] \times \mathbf{g}^j_{a_j}[i] = \mathbf{z}^j_{a_j}[i], \quad (6)$$

III. Algorithmic Alternatives

As mentioned in the previous section, there are many algorithmic options for QRD. Given Rotations, Householder Reflections and Gram-Schmidt orthogonalization are the more important methods to perform QRD.

Householder reflection is a matrix of the form $\mathbf{H} = \mathbf{I} - 2uu^\tau/(u^\tau u)$. It is the generalization of the reflection onto the plane with normal vector $u \in \mathbf{R}^n$.

With a given vector $x \in \mathbf{R}^n$ and $x \neq \mathbf{0}$, we can find a householder reflection $\mathbf{H} = \mathbf{I} - 2uu^\tau$ to zero out all but the first entry of x, that is $\mathbf{H}x = \begin{bmatrix} c & 0 & \ldots & 0 \end{bmatrix}^\tau = ce_1$.

Let $u = x + ce_1$, then we can get $u^\tau x = x^\tau x + cx_1$ and $u^\tau u = x^\tau x + 2\alpha x_1 + \alpha^2$, this will produce

$$\mathbf{H}x = (1 - 2\frac{x^\tau x + \alpha x_1}{x^\tau x + 2\alpha x_1 + \alpha^2})x - 2\alpha \frac{u^\tau x}{u^\tau u} e_1. \quad (7)$$

In order to satisfy $\mathbf{H}x = ce_1$ we set $\alpha = \pm \| x \| e_1$, then

$$u = x \pm \| x \| e_1 \rightarrow \mathbf{H}x = (\mathbf{I} - 2\frac{uu^\tau}{u^\tau u})x = \mp \| x \| e_1, \quad (8)$$

Denote the $\mathbf{a}_i$ as the i^{th} column of matrix $\mathbf{A}$, $\mathbf{A}_1 = \mathbf{H}(\mathbf{a}_1)\mathbf{A}$ will have the first column of $\mathbf{A}_1$ being zeros except the first element $a_{1,1}$. By repeating householder reflections, we can transform $\mathbf{A}$ into an upper-triangular matrix $\mathbf{H}_{n-1}\mathbf{H}_{n-2}\ldots\mathbf{H}_2\mathbf{H}_1\mathbf{A} = \mathbf{R}$ with $\mathbf{Q} = \mathbf{H}_1\mathbf{H}_2\ldots\mathbf{H}_{n-2}\mathbf{H}_{n-1}$.

We define rotations in $\mathbf{R}^n$ by the following given rotation matrix:

$$\mathbf{G} = \begin{bmatrix} 1 & & & & & \\ & \ldots & & & & \\ & & c^* & & s^* & \\ & & & \ldots & & \\ & & -s & & c & \\ & & & & & \ldots. \\ & & & & & 1 \end{bmatrix}, \quad (9)$$

where the $c = \cos\theta$ and $s = -\sin\theta$ appear in the i th and j th columns and all other entries are 0 or 1. This is called Given Rotation. For a given matrix $\mathbf{A}$ with $a_{ii} = x$ and $a_{ji} = y$, we can let

$$c = \cos\theta = \frac{x}{\sqrt{\| x \|^2 + \| y \|^2}}, s = -\sin\theta = \frac{-y}{\sqrt{\| x \|^2 + \| y \|^2}}$$

and $\mathbf{GA}$ will have the (j,i) element being zero. By cascading a series of given rotation matrix together, the matrix $\mathbf{GA}$ will be transformed to an upper triangular matrix $\mathbf{G}_N\mathbf{G}_{N-1}\ldots\mathbf{G}_2\mathbf{G}_1\mathbf{A} = \mathbf{R}$. The $\mathbf{Q}$ in $\mathbf{A} = \mathbf{QR}$ is then calculated as $\mathbf{Q} = \mathbf{G}_N^\tau\mathbf{G}_{N-1}^\tau\ldots\mathbf{G}_1^\tau$. Since the $\mathbf{G}$ in each step is orthogonal, the $\mathbf{Q}$, as the product of conjugated orthogonal matrixes, is still orthogonal. With GR method, we can decompose $\mathbf{A}$ into two specific matrix $\mathbf{Q}$ and $\mathbf{R}$.

In most scientific and signal processing libraries QRD is implemented with Householder Reflection [11]. This is motivated by the abstract complexity analysis which concludes that Householder Reflection has the highest efficiency. However, we choose Given Rotation in our work, because we discover that Given Rotation can considerably outperforms Householder Reflection after removing the redundancy. In addition, it is easier to remove the redundancy with Given Rotations based QRD.

IV. The Redundancy Removal

As we can see in the previous section, the GR based QRD is essentially a series of matrix multiplications and conjugated matrix multiplications. Since matrix multiplication has high complexity, comprehensive optimization is necessary.

Although the formulations explicitly and clearly present mathematical meanings of Given Rotation, the direct implementation of the formulations will contain lots of redundancies. We observe two categories of redundancy in the

SRI-RLS, the first is applicable for all QRD based algorithms, and the second is specific for the SRI-RLS.

A. The Redundancy Removal for Generic QRD

First we remove the redundancy at the level of mathematical operations. We can observe that the QRD updating in SRI-RLS is only for triangularization. Since the coefficient vector $\mathbf{g}_{a_j}^j[i]$ is solved from $(\mathbf{R}_{a_j}^j[i], \mathbf{z}_{a_j}^j[i])$ that are actually part of the triangular matrix (output of QR), the $\mathbf{Q}$ is not involved in any computation afterward. Hence, we can remove the $\mathbf{Q}$ related operations.

The aforementioned redundancy removal is feasible in only Given Rotation. On the contrary, in Householder Reflection and Gram-Schmidt method, the intermediate $\mathbf{Q}$ is involved in complex dependencies, so that related computations can not be removed.

Another redundancy we observe at the mathematical operation level is in the triangularization itself. The matrix multiplication $\mathbf{GA}$ is to make the element $a_{i,j}$ of $\mathbf{A}$ to be zero. Since the given rotation matrix $\mathbf{G}$ has specific structure as that in Eq.(9), the computation $\mathbf{GA}$ can be greatly simplified. In addition, Since the indexes (i, j) change in an incremental way, when performing the multiplications to zero-out $a_{i,j}$, the matrix to rotate already has a part being zeros:

$$\begin{bmatrix} a_{j,1} & \dots & a_{j,j-1} \\ a_{i,1} & \dots & a_{i,j-1} \end{bmatrix} = [\mathbf{0}] \tag{9}$$

Hence, we should further remove the redundancy in the in $\mathbf{GA}$ and greatly simplify it as:

$$\begin{bmatrix} a_{j,j} & \dots & a_{j,N} \\ a_{i,j} & \dots & a_{i,1} \end{bmatrix} \leftarrow \begin{bmatrix} c^* & s^* \\ -s & c \end{bmatrix} \begin{bmatrix} a_{j,j} & \dots & a_{j,N} \\ a_{i,j} & \dots & a_{i,1} \end{bmatrix}. \tag{10}$$

The two simplifications significantly reduce the complexity of the multiplication $\mathbf{GA}$.

After removing the redundant operations at mathematical operation level, we also remove the redundancy at implementation level. The most important redundancy is address generation. We observe that half of the Function Units (FUs) of VLIW Digital Signal Processor (DSP) are occupied by address calculation in the original implementation. In fact, the memory access in Given Rotation is highly regular and predictable. Hence, we explicitly use memory pointers which increase by strides. This optimization significantly reduces the amount of address calculations.

B. The SRI-RLS Specific Redundancy Removal

After removing redundancy that is generic for all QRD based algorithms, the structure of SRI-RLS is then studied to achieve further optimization for QRD implementation. From Eq.(2), it is clearly seen that the input to QRD is a matrix with deterministic structure. Specifically, since the linearly scaled version of the previously triangulated matrix $\mathbf{R}$ is part of the new input to QRD and the newly received information $[\mathbf{Y}_{a_j}[i-1]\mathbf{C}_p^j[i]^{\mathrm{H}} \quad s_p^j[i]]$ is the row-vector to zero-out. Furthermore, from the structure in Eq.6, we can see that each single give rotation operation in $\mathbf{G}_N\mathbf{G}_{N-1}...\mathbf{G}_2\mathbf{G}_1\mathbf{A}$ will change only two rows. This implies that a full QRD is not needed. We need to perform given rotation for only the bottom element of each column.

Comparing to other QRD algorithms, it is very easy to incorporate extensions to remove the aforementioned redundancy in Given Rotation. In Given Rotation, since the down-triangle elements are eliminated one-by-one, the redundant rotations can be removed in a simple and efficient way. In contrast, Householder Reflection rotates the whole column instead of a single element as what Given Rotation does. Since the probability of having an all-zero column is extremely low, the potential for redundancy removal is much lower than Given Rotation. Similarly, it is very difficult to incorporate extensions to remove this kind of redundancy in Gram-Schmidt method.

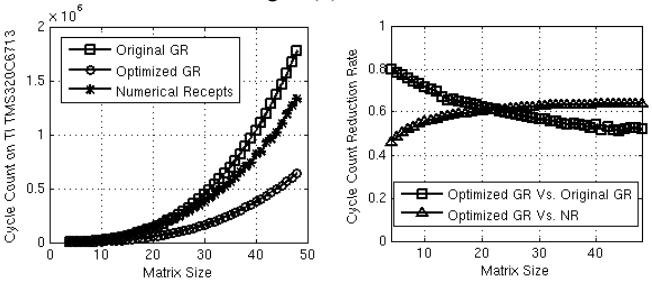
V. IMPLEMENTATION GAIN ON TMS320C6713

The experiments are performed on TMS320C6713, a typical VLIW DSP as those seen in many SDR platforms [12][13]. Because the memory access in the SRI-RLS is highly deterministic and predictable, L2 memory of the TMS320C6713 is configured as SRAM. Compilation and Profiling are performed in TI Code Composer Studio with the highest optimization level.

In our work, the cycle-count on TMS320C6713 is considered as the cost of implementation. We compare the optimized implementation to the original implementation (directly translated from mathematical formulations). In addition, we compare our work to the widely accepted QRD implementation given by Numerical Recipes [9], which is often considered as one of the most important references.

A. The Redundancy Removal for Generic QRD

Since the input matrix $\mathbf{A}$ of QRD has different sizes for different channel cases, we study a practical range [4,48]. The cycle-count comparison is shown in Fig.1 (a). In order to have a quantitative view on the improvement, we plot the cycle count reduction rate in Fig. 1 (b).



(a) (b)

Fig.1. Results of The Generic Redundancy Removal in QRD. (a) Cycle-count of Different QRD Implementations on TMS320C6713. (b) Reduction Rate.

It is clearly shown in Fig.1 that the removal of the redundancy in QRD brings significant gain. Comparing to both of the two references (the original implementation and

the implementation in Numerical Recipes), the average cycle count reduction rate is above 60%.

Moreover, we study the memory subsystem performance. Since L2 memory is configured as SRAM, we focus on the performance of L1. The results are shown in Table.1, where the number of CPU stalls on L1D (L1 data cache) and L1P (L1 instruction cache) is listed for different matrixes. We can see that our proposal achieves magnitudes of gain in Level 1 memory access. Since modem DSPs often have a complex L1 memory and very wide cache lines, the improvement brings both significant cycle-count and energy reduction.

Table 1. Level 1 Memory Performance Comparison

N	Implementation	CPU.stall.mem.L1D	CPU.stall.mem.L1P
12	Original GR-QRD	114	1673
	Numerical Recipes	18	1464
	Our work	1	44
24	Original GR-QRD	699	6716
	Numerical Recipes	51	5112
	Our work	108	40
48	Original GR-QRD	42320	27161
	Numerical Recipes	77691	18572
	Our work	10212	40

A. SRI-RLS Specific Redundancy Removal

In order to make a comprehensive investigation, we verify the SRI-RLS specific redundancy removal for a set of representative channel cases. We study channel cases specified in ITU-R M.1225 [6], 3GPP TR 25.943 [5] and 3GPP TS 25.101 [14]. The channel cases are listed in Table 2.

Table 2. Channel Cases

Channel Case	1	2	3
Name	3GPP 1	3GPP 3	3GPP 4
Channel Case	4	5	6
Name	3GPP 5	3GPP 6	ITU Ped. A
Channel Case	7	8	9
Name	ITU Ped.B	ITU Veh.A	COST259 TU
Channel Case	10		
Name	COST259 RA		

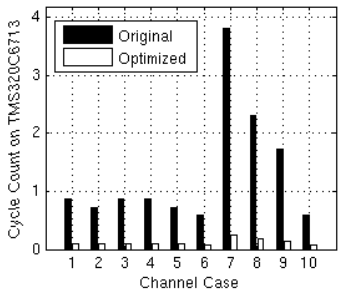


Fig.2. Cycle Count Reduction of SRI-RLS Specific Redundancy Removal

The results are shown in Fig.2, where the cycle counts of different implementations are plotted with different bars. From the figures we can conclude that the gain of removing SRI-RLS specific redundancy is also remarkable. Specifically, the average cycle count reduction rate of the 10 cases is 89.93%.

VI. CONCLUSIONS AND FUTURE WORK

In this paper, we introduced the optimizations for QRD implementation in SRI-RLS based HSDPA chip level equalization. Based on systematic and comprehensive redundancy removal, our work achieves remarkable gain over the widely accepted QRD implementation in Numerical Recipes. Since the SRI-RLS specific removal is orthogonal to the redundancy removal in generic QRD, the gain achieved by the two steps is the product of the gain in each step. Hence, comparing to the implementation in Numerical Recipes, the average cycle-count reduction rate achieved by our proposal is $1-(1-0.63)(1-0.893)=0.964=96.4\%$.

SRI-RLS represents a large family of advanced algorithms utilizing square root information, orthogonal transformation or projection principles. Hence, the principles and methods could be applied to similar algorithms. Since modern statistical signal processing techniques largely rely on cascaded matrix operations, the redundancy should be carefully studied to enable efficient programmable implementations.

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