A FRAME-START DETECTOR FOR A 4×4 MIMO-OFDM SYSTEM

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ABSTRACT

Future wireless LANs will increase the peak data rate by employing multiple antennas at both transmitter and receiver.

Well designed synchronization algorithms are a prerequisite for meeting stringent QoS requirements. In particular OFDM modulation, which constitutes the basics for WLAN, is very sensitive to timing synchronization errors which incur inter-symbol interference. In this paper, a novel frame synchronization algorithm is proposed that is implemented in the FPGA of a real-time MIMO-OFDM testbed. Simulations show it to be of sufficient performance in scenarios of interest, while the hardware complexity is suitable for an FPGA implementation. Additionally, the algorithm exhibits a good resilience against narrow-band interference, which causes problems in traditional frame-start detection algorithms.

1. INTRODUCTION

Multiple-input multiple-output (MIMO) systems [1] employ multiple antennas at both transmitter and receiver in order to significantly improve link reliability and throughput of wireless communication systems. These gains come at no additional transmit power or bandwidth expenditure.

IEEE 802.11a [2] is an established WLAN standard that provides data rates of up to 54 Mbps, using single-input single-output (SISO) antenna technology, and employing orthogonal frequency division multiplexing (OFDM) modulation.

The use of OFDM drastically simplifies equalization, and consequently, receiver design. MIMO technology in combination with OFDM is therefore expected to constitute the basis for the upcoming IEEE 802.11n standard, which extends IEEE 802.11a to higher data rates by using up to four antennas at both transmitter and receiver. MIMO gains however can only be realized if both frequency and timing synchronization are realized properly. Implementations of WLAN synchronizers based on correlation parameters [3] have been presented in [4, 5, 6]. However, these algorithms are prone to narrow-band interference as shown in [7]. Alternative solutions employing matched filtering exhibit a silicon complexity that is often prohibitively high.

Contributions: A novel frame-start detection algorithm for MIMO-OFDM is presented. It is based on the observation of the estimated signal power with subsequent post processing. The performance of the implemented frame-start detector (FSD) is evaluated with computer simulations. It is shown to be sufficient for practical indoor scenarios. The silicon complexity is shown to be low by a real-time FPGA implementation.

Outline of the paper: Sec. 2 describes the system architecture and the structure of the MIMO-OFDM radio frames. In Sec. 3 the automatic gain controller (AGC) is introduced, which constitutes the basis for our proposed FSD. In Sec. 4 the principle of the FSD algorithm is detailed. The corresponding performance is evaluated through simulations in Sec. 5. Implementation results and conclusions are presented in Sec. 6 and Sec. 7.

2. MIMO-OFDM SYSTEM MODEL

We consider a 4×4 MIMO-OFDM system with four spatially multiplexed data streams ($m \in \{1, 2, 3, 4\}$) as outlined in Fig. 1 and as described in [8]. The kth OFDM symbol in frequency domain can be described as a $4 \times N$ matrix $\mathbf{S}^{(k)}$, where $N = 64$ is the number of OFDM tones, according to the IEEE 802.11a standard. After OFDM modulation, IFFT, and cyclic prefix (CP) insertion, the signal is digitally up-converted (DUC) to 20 MHz and D/A converted. Subsequently, the signal is transmitted by the RF subsystem at 2.4 GHz. The RF part of the receiver applies the real-valued signal at an intermediate frequency of 20 MHz to the 80 MSps A/D converter. The AGC controls the signal power in both the digital and analog domain. Following the A/D converter, $\widetilde{r}_m[t]$ is amplified digitally for the subsequent digital down conversion (DDC). After frequency offset compensation (FOC) and FSD with CP removal the OFDM symbols

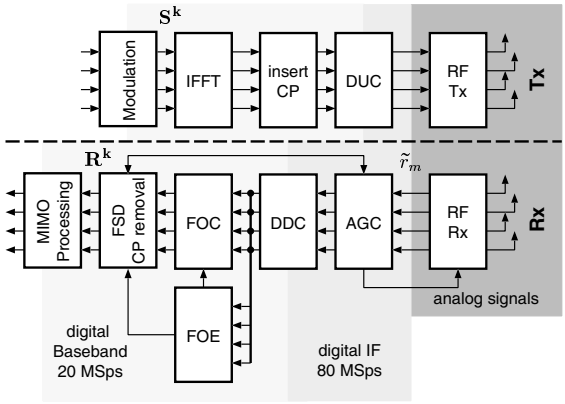

Fig. 1. System overview over a MIMO-OFDM system physical layer without coding.

$\mathbf{R}^k$ are applied to MIMO algorithms that aim at estimating the transmitted data signals. Note that the proposed frame start detector can also be employed in systems that obtain I/Q demodulated baseband signals from the A/D converters.

Frame Format: The employed frame structure is based on the IEEE 802.11a standard. It is comprised of preamble, MIMO training and data symbols. The preamble is used for frame-start detection and frequency offset estimation (FOE). Channel estimation is performed with the aid of the MIMO training symbols. Finally, the data streams that are spatially multiplexed follow the MIMO training. The FSD operates on the first part of the preamble, called short preamble, which corresponds to the first two of totally four OFDM preamble symbols. The short preamble OFDM symbols occupy every fourth tone resulting in a 16 baseband sample periodicity. While the first antenna transmits the original IEEE 802.11a short preamble, the others transmit the same signal, but scrambled with a Hadamard sequence in the frequency domain. This scheme avoids unintended beam forming and thus large errors in the power estimation at the receiver. Note that the proposed FSD scheme will also work for the frame format currently proposed in the IEEE 802.11n standard.

3. AUTOMATIC GAIN CONTROL (AGC)

OFDM communication systems exhibit a high peak-to-average power ratio (PAPR) which increases the importance of AGC. In MIMO systems, the PAPR is not significantly enlarged compared to the SISO case and the PAPR does not exceed 10.5 dB in 0.1 % of the frames. The AGC controls the signal power in order to avoid overflows at the A/D converters and to optimally exploit the dynamic range of the digital baseband processing part. The signal power is controlled at each antenna individually. An overview of the AGC is given in Fig. 2.

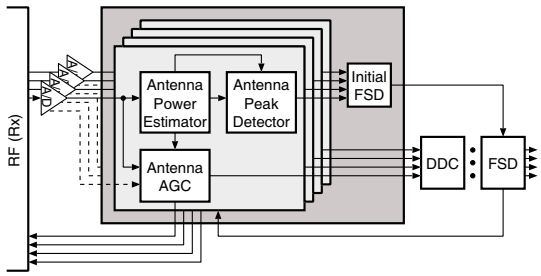

Fig. 2. Overview of the AGC (dark grey box) which is composed of four per-antenna independent AGCs, power estimators, and peak detectors and one initial FSD block.

Antenna Power Estimator (APE): To obtain the instantaneous signal power $\widetilde{p}[t]$, a multiplier is employed to square the input signal (see Fig. 3). The average received power estimate $\widehat{p}[t]$ is produced by a first order IIR filter according to $\widehat{p}[t] = \tau\widetilde{p}[t] + (1-\tau)\widehat{p}[t-1]$ with $\tau = \frac{1}{64}$. τ is chosen such that the signal power of the 64-sample periodic preamble can be calculated both accurately and fast. Once a frame start is detected, the antenna power estimators are frozen such that no change in the AGC settings may occur during frame reception.

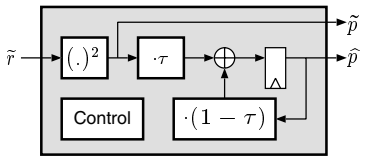

Fig. 3. Antenna power estimator employing one multiplier and an IIR filter with τ being a negative power of two.

Antenna AGC: The AAGC (see Fig. 4) controls the signal power at the input of the A/D converters, making use of a digitally controllable attenuator in the RF part of the receiver. To obtain faster settling times, an over-range signal provided by the A/D converter is used which instantly causes the variable attenuator in the RF chain to be set to a high value. Additionally, the signal amplitude at the input of the DDC is

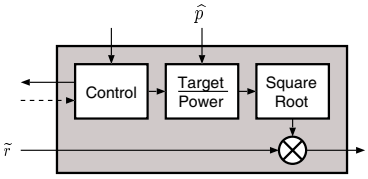

Fig. 4. Overview of the AAGC which is composed of a serial division block, a serial square root block, a multiplier, and a controller.

amplified digitally if the analog signal power is below optimum values. The corresponding factor is obtained with $\sqrt{\frac{p_t}{\widehat{p}}}$, where p_t defines the target power.

4. FRAME-START DETECTION ALGORITHM

The frame start detection is based on the observation of the power levels on all antennas. The exact timing of the frame start event is obtained from a simultaneous power increase on multiple antennas in order to reduce the frame false detection probability. A frame start is confirmed only if the power level remains higher compared to the pre-event power level over a substantial time period. Three blocks cooperate to execute the algorithm as outlined below:

Antenna Peak Detector (APD): Each antenna is equipped with a peak detector, as shown in Fig. 5, which has two modes. The *peak detection* mode focuses on the detection of short-term power peaks while the *power increase* mode is used to detect long-term power level changes on the antenna. In *peak detection* mode, the instantaneous signal power $\widetilde{p}[t]$ is compared to the estimated signal power $\widehat{p}[t]$. The output of the comparator ($v[t]$) is given by calculating

$$\begin{cases} v[t] = 1: & \widetilde{p}[t] > \alpha \cdot \widehat{p}[t] \\ v[t] = 0: & otherwise. \end{cases} \quad (1)$$

The peaks detected in (1) are subsequently widened in time to increase the subsequent initial frame start detection probabil-

ity:

$$\begin{cases} w\,[t] = 1: & \sum_{k=0}^{\beta-1} v\,[t-k] > 0 \\ w\,[t] = 0: & otherwise. \end{cases} \quad (2)$$

$w[t]$ is fed to the initial FSD block. In our case, both $\alpha, \beta = 2$. Higher values for α increase the frame miss probability in low SNR regimes but decrease the false alarm rate. If a peak at the antenna is observed at time instant t_p (i.e. $w[t_p] = 1$), the current average power estimate $\widehat{p}[t_p]$ is stored and the *power increase* mode is initiated.

In the *power increase* mode, $v[t]$ is obtained by replacing $\widetilde{p}\,[t]$ with $\widehat{p}\,[t]$ and $\widehat{p}\,[t]$ with $\widehat{p}\,[t_p]$ in (1). Normal *peak detection* mode is not resumed for 128 subsequent samples in order to observe the signal during a substantial part of a potential frame start. Thereafter, $v[t] = 0$ causes the APD to return to the *peak detection* mode. If $v[t] = 1$ for more than an additional 256 samples, *peak detection* mode is also resumed. This is to avoid a lock of the APD on an antenna in case of a sustained power increase due to an interferer.

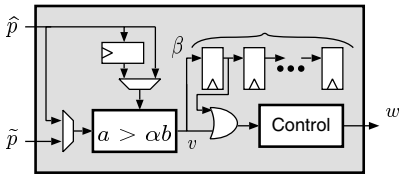

Fig. 5. Antenna peak detector circuit.

Initial Frame-Start Detection (IFSD): The IFSD operates on the four output signals of the antenna peak detectors $w_k[t]$. A significant power peak is detected by detecting a simultaneous peak on at least three of the four receive antennas.

$$\begin{cases} f\,[t] = 1: & \sum_{k=1}^{4} w_k\,[t] > 2 \\ f\,[t] = 0: & otherwise. \end{cases} \quad (3)$$

Frame-Start Detection (FSD): The actual FSD algorithm is given in Fig. 6 and operates on the $f[t]$ signal and its recent history. The algorithm first detects the timing of a frame with an initial power increase. The frame start is later confirmed definitely only if the power increase is sustained. The

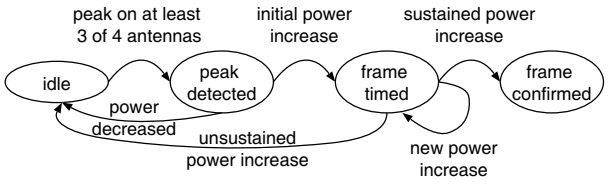

Fig. 6. State diagram of the proposed FSD algorithm.

implementation of the frame-start detection consists of an accumulator that reflects the history of $f[t]$ and a controller (see Fig. 7). The accumulator calculates $A[t] = \sum 2(f[t] - 0.5)$. The value $A[t]$ is saturated such that only values $\{0, 1, \ldots, 255\}$ occur. The absolute timing of a frame start is tentatively detected if $A[t] = 4$ and $A[t-1] = 3$. Other frame timing events are ignored if they occur within a 64 samples window from the tentative detection. This is to avoid errors in the frame timing due to initial power fluctuations at the antennas. Only if the accumulator reaches 127 within 255 samples, the tentative frame detection is confirmed. This is to avoid false detections caused by short signal power bursts. Additionally, the correlation parameters described in [3] may be considered to obtain a second confirmation of the frame detection. However, this is not included in the performance simulations presented in the next section as the benefit of correlation based synchronization in the case of narrow-band interferer is limited due to the inherent correlation properties of the interferer.

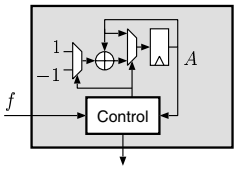

Fig. 7. Frame-start detection circuit consisting of a controller and an accumulator.

5. FSD PERFORMANCE SIMULATIONS

In order to assess the performance of the proposed algorithm, the results of a fixed-point simulation are evaluated.

Simulation Parameters: Fig. 8 outlines the simulation. At the transmitter, the complex-valued 20 MSps baseband preamble in the time domain is sent through a 4×4 MIMO channel with 1 to 4 sample spaced taps with equal power. This model covers typical indoor scenarios. Subsequently, the signal is digitally up-converted to a real-valued 80 MSps signal with a center frequency of 20 MHz. The signal is then conditioned such that the signal power is constant for all receive antennas and channel instances according to the current receive SNR setting. Wide band thermal noise is added to the signal at digital IF. A narrow-band interfering signal is optionally be added

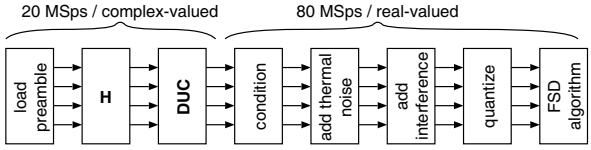

Fig. 8. Simulation model.

according to the current receive SIR setting. In-band interference is assumed, thus the frequency of the narrow band interferer is chosen randomly between 1 MHz and 39 MHz per channel instance. The quantizer produces a signal with a range corresponding to the A/D converter. A frame is considered to be correctly synchronized if the detection time falls within the inter-symbol interference free part of the cyclic prefix.

Simulation Results: In Fig. 9, the performance was evaluated at different SNR levels ranging from 4 to 10 dB. Beyond 7 dB the frame detection probability is above 90%. No false frame detection was observed after simulating a real-time interval of 2 seconds.

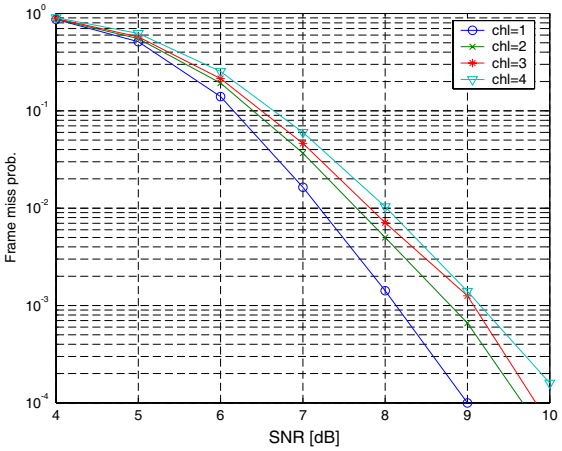

Fig. 9. Received SNR sweep vs. frame miss probability at different channel lengths over 50,000 channels and frames.

In Fig. 10, the thermal noise level was set 20 dB below the received signal power level. An in-band narrow band interferer disturbs the signal at various signal-to-interference ratios (SIR). The simulation shows a good resilience to narrow band interferer. False detections may only occur if narrow band interferers with frequencies below the cut-off frequency of the low-pass IIR filter in the power estimator disturb the signal. This is caused by low-frequency fluctuations of the power estimate $\widehat{p}$.

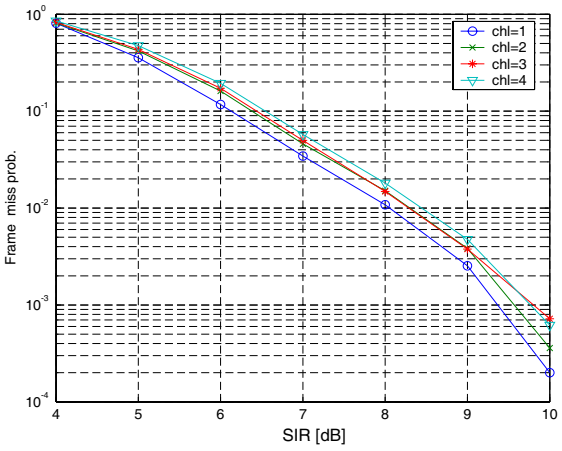

Fig. 10. Received SIR sweep vs. frame miss probability in the presence of narrow band interference at different channel lengths over 50,000 channels and frames.

6. IMPLEMENTATION RESULTS

The algorithm has been implemented on Virtex-2 1000-4 FPGAs. The system clock is 80 MHz. Resources used by the relevant blocks are summarized in Table 1. Most blocks are instantiated four times due to the 4×4 MIMO setup.

Table 1. Area usage of the FPGA FSD implementation

Component	Slices	Multipliers
4x Power Estimator	456	4
4x Peak Detector	252	0
4x Initial Frame-Start Detector	4	0
Frame-Start Detector	24	0
Total Frame-Start Detector Circuitry	736	4

7. CONCLUSIONS

A real-time FPGA implementation of a frame-detection algorithm for a 4×4 MIMO-OFDM system was presented. The realized implementation of the frame detection algorithm occupies a total of 736 slices and 4 multipliers on Virtex-2 FPGAs. It has been shown through simulation that the algorithm performs well in indoor environments, even in the presence of narrow band interference. Only, bursty interferers or extremely-low-frequency narrow-band interferers with significant signal power can cause false frame detections.

8. REFERENCES

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