Analysis and Design of Voltage Regulator with Improved Light Load Efficiency

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***Abstract*— A Voltage Regulator (VR) design with improved efficiency especially at light load and with good steady-state ripple and dynamic performance is discussed in this paper. The presented VR utilizes a proposed "Pulse-Sliding*" load adaptive control scheme to satisfy the VR requirements. Such VR design is important in many applications including those that are battery powered and has energy consumption constrains. In this paper, the concept, design, analysis, simulation and experimental circuit of the improved VR design are presented.**

I. INTRODUCTION

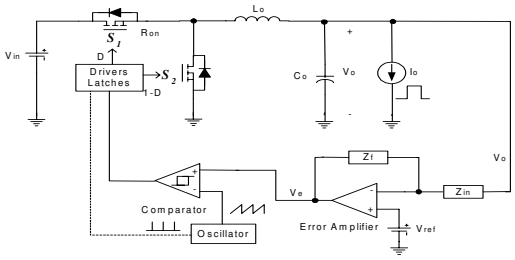
Unlike many Voltage Regulator (VR) applications where achieving high efficiency toward the full load is the most important factor (even at the expense of lower light loads efficiency), mainly to avoid thermal issues, in other applications such as those that are battery-powered and have constrains in energy consumption, high efficiency at all load conditions including light load is required. [1,2]. For such applications, this becomes even more important when the load operates at different power/current demands depending on applications or usage conditions such as DSP (Digital Signal Processor) ICs (Integrated Circuits) used in the applications of portable computers and handheld devices.

Figure 1 shows an example VR efficiency curve that does not use special efficiency improvement technique at lighter loads. In order to "flatten" such efficiency curve and improve light load efficiency, several techniques can be adapted such as the so called Mode-Hopping and Pulse Skipping [1,2]. In Mode-Hopping technique, the DC-DC Buck VR, for example, operates in synchronous mode at CCM (Continuous Conduction Mode) at high load demands while the inductor current does not go below zero, and operates in asynchronous mode at DCM (Discontinuous Conduction Mode) when the inductor current start approaching the zero amperes point to reduce mainly conduction losses [1,2]. While in Pulse-Skipping or variable switching frequency technique the VR switching frequency is lowered as the load becomes smaller to reduce mainly switching losses and can be implemented by using hysteretic control or variable frequency PWM control. Both techniques result in efficiency improvement especially at light load, however, at increased current/voltage ripple and possible effect on dynamic and steady-state performances, which are important for many IC loads especially those powered by low voltage and are highly integrated.

In this paper, a non-linear variable frequency load adaptive control concept, namely "Pulse-Sliding" control is proposed and the design, analysis, and experimental work of a VR with improved efficiency and steady-state and dynamic performances is presented.

Next section briefly discusses the VR power losses trends. Section III reviews some of the light load efficiency improvement techniques with loss analysis followed by Section IV that presents the Pulse-Sliding technique of this paper. Section V presents the VR dynamic performance while Section VI discusses the Pspice/Orcad simulation results and future experimental work. The conclusion is given in Section VII.

* Patent Pending



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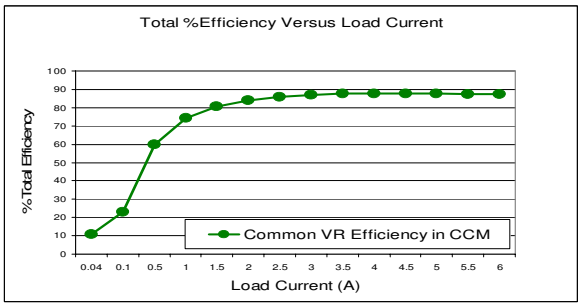


(b)

Fig. 1: DC-DC buck VR and example efficiency curve

II. VR POWER LOSSES STUDY AND TRENDS

A. *VR Losses Sources Quick Overview*

The conduction loss is one type of the VR power losses. This type is as a result of components parasitic resistances such as the switch R_{DS-ON}, the capacitors ESR, the Inductor DCR, and the sense and traces resistances. This loss is a function of the load current and the *rms* value of the VR currents (function of current ripple) which is controlled by several factors including the switching frequency, the inductor value, and the input-to-output voltage ratio. The hard-switching loss is another type of VR power losses as a result of the voltage-current overlap period during switching and is a function of the switching frequency and the switches' parasitics values. The reverse recovery loss is another power loss type that is a function of the switching frequency and the switch reverse recovery charge in addition to the voltage applied across the switch. The gate drive loss is a VR loss that is also a function of the switching frequency in addition to the applied gate drive voltage and switch gate charge. Other VR power losses include inductor/magnetic components core losses and leakage currents and standby losses. VR power losses Equations can be found in the literature such as those presented in [2] and they were not included here because of the space limitation.

B. *Power Losses Effects as a Function of the Load*

VR power losses effect become more significant as load becomes lighter because they become larger portion of the output power drawn

by the load, which greatly degrades the VR efficiency. One important reason of this is that the switching frequency dependent losses including the hard-switching and gate drive losses do not scale much with the load. Fig. 2 shows an example of how VR power losses percentages (P_{Loss}/P_o) tend to be as a function of the load for a fixed frequency PWM buck converter in CCM mode. It can be noticed that at some load point, the hard-switching and gate drive losses total to be larger than the actual power delivered to the load.

III. Light Load Efficiency Improvement Techniques Study

As mentioned earlier, Mode-Hopping (MH) or/and Pulse Skipping (PS) are techniques used to improve light load efficiency. In this section, the advantages and disadvantages of such techniques are briefly discussed to follow of proposed modified control method in the next section.

The discussion will base on the following buck VR design example: $V_{in} = 5V$, $V_o = 1V$, $L_o = 0.47\mu H$, $C_o = 250\mu F$, and $f_{sw} = 250kHz$. In the analysis, the switches specifications used are for IRF6633 for the control FET and IRF6619 for the Synchronous FET. The resistances DCR, R_{sense} , and ESR are taken to be equal to $4m\Omega$, $4m\Omega$, and $3m\Omega$, respectively.

A. *Mode-Hopping Steady-State Effects*

Operating at DCM mode once the inductor current tries to go negative will result in some efficiency improvement because of: 1) Lower conduction losses when operating way deep in DCM (very light load) since ripple current and *rms* currents are reduced, and 2) Some hard-switching losses are saved for example because the control (upper) switch current is zero when it is turned ON. Fig. 3(a) shows the VR power losses percentages while operating at fixed frequency PWM with MH, which can be compared with Fig. 2 losses.

Unfortunately, the output voltage ripple increases at the CCM-DCM transition and is reduced again as the load becomes lighter as shown in Fig. 3(e), which may exceed supply voltage deviation required by the load and increase the ESR power loss.

B. *Pulse-Skipping or Variable Frequency Effects*

Decreasing the switching frequency at lighter loads will further improve the lighter loads efficiency especially while operating at DCM (MH) at the same time, as shown in Fig. 3(b), because of the reduction in hard-switching and gate-drive power losses which has more significant effect on efficiency compared to the conduction loss. Moreover, the output voltage ripple will also increase to be sometimes higher or same compared with using MH without PS, depending on the design.

C. *Statement Regarding Techniques Effects*

The amount of efficiency improvement and output ripple increase is a function of many parameters including input voltage, output voltage, switching frequency, inductor value, and components parasitics. For example, when the input voltage is higher for the same output voltage, the output voltage ripple increase when using MH and PS will be even higher even though the efficiency improvement is more significant compared to the buck VR without MH and/or PS. Another note is that the effect of efficiency improvement techniques on steady-state and dynamic performance should be studied. Dynamic performance evaluation will be briefly discussed (because of space limitation) later on in this paper.

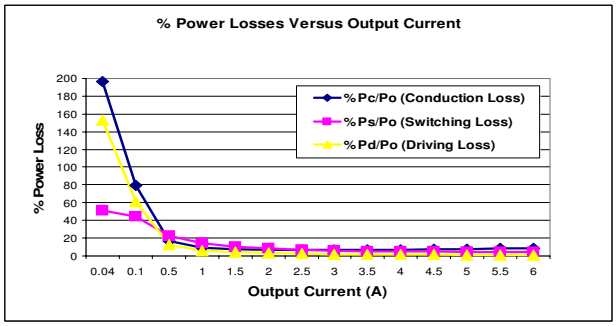
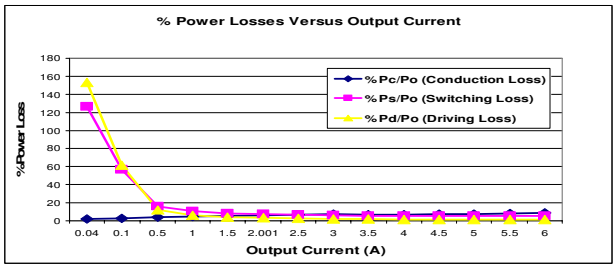


Fig. 2: Example of CCM Buck VR Power Losses Percentage as a Function of the Load.



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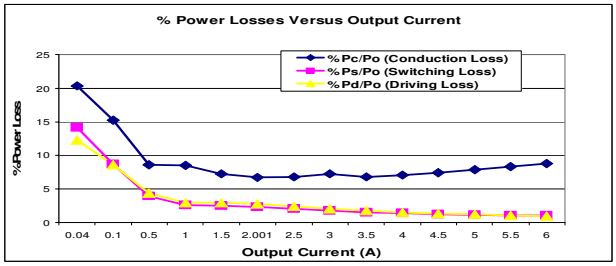

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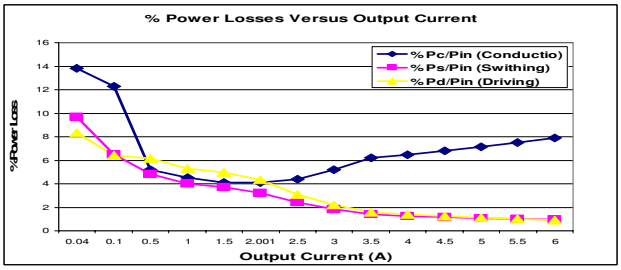

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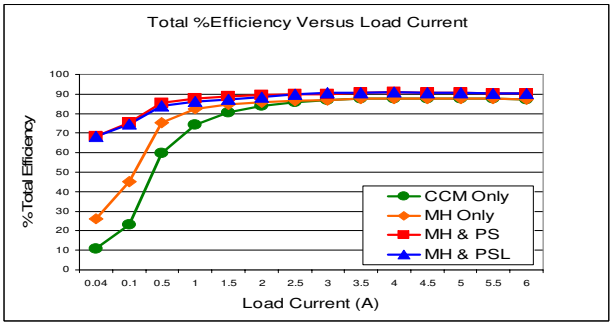

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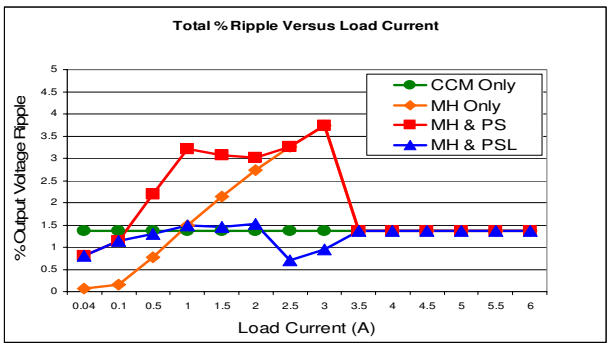

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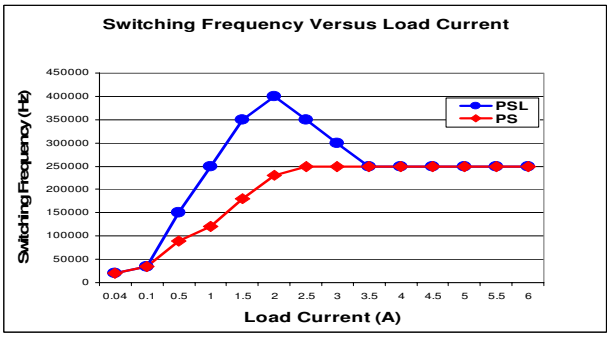


(f)

Fig. 3: Power Losses and Efficiency Analysis for Different VR Cases

IV. Proposed Pulse-Sliding Technique

In this section, a non-linear variable frequency technique, namely Pulse-Sliding (PSL) is presented to improve the VR efficiency at lighter loads while keeping low steady-state ripple at light loads without the need to add larger output capacitance and to be able to maintain good dynamic performance. Moreover, this technique, in its implementation concept, utilizes a way to eliminate the abrupt transition between the operation modes.

Fig. 4 shows the PSL operation concept, where the VR operates under fixed nominal f_{sw} and CCM at high loads. Then, f_{sw} may have to be initially increased when switching to DCM at lighter loads in the CCM-DCM transition region to maintain low voltage deviation before f_{sw} is decreased below the nominal at very light loads as the VR starts to operate far from the transition region and the ripple starts to drop. Increasing f_{sw} during the transition will result in some additional switching losses during the transition period but will save conduction losses, which may not result in lower efficiency, as shown in Fig. 3(c). Fig. 3(e) and Fig. 3(f) shows ripple and efficiency comparisons between the proposed PSL technique and the other techniques. The PSL technique results in lower ripple and with high efficiency.

Fig. 5 shows an example analog implementation circuitry of the proposed controller (Can be also implemented as a digital control program). S_{Li} and S_{Hi} are the synchronous complementary PWM control signal by the PWM generator while S_{LF} and S_{HF} are the final PWM control signal that will drive the Buck VR low-side and high-side switches, respectively. Note that Fig. 5 is for operation concept demonstration and that actual and final implementation circuit may differ.

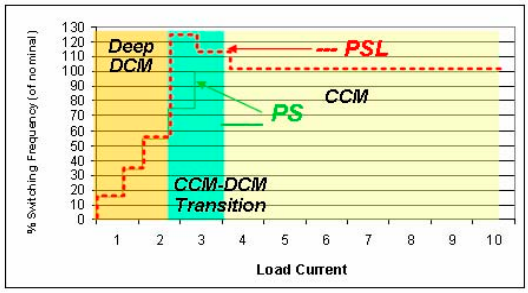


Fig. 4: Proposed Pulse-Sliding Concept

The inductor current is sensed to detect when it tries to go below zero by comparator comp #1 that will go output high and reset SR #1 to force DCM mode by forcing S_{LF} to go low. SR #1 is set again at the next switching cycle by the OR-gate. SR #2 generates the high-side switch control S_{HF} ; it is set by S_{Hi} and reset by an AND gate output that will go high if both comp #2 output is high and SR #3 is set. Comp #2 output will go high if the inductor current peak exceeded certain maximum value $V_{L\max-DCM}$ in DCM and SR #3 will be set only when comp #1 output is high, which means that the current mode is DCM. Therefore, the peak current limit will be only active in DCM mode to maintain certain output voltage ripple. SR #3 will be reset each time SR #1 is set by S_{Li} or by the AND-gate output. This is because whenever SR #2 is reset in DCM to force S_{HF} to go low and prevent inductor peak current to exceed the limit, SR #1 should be set to provide a path for the inductor current.

S_{Li} and S_{Hi}, generated by the PWM generator, will control the VR switching frequency in both CCM and DCM modes. The PWM generator frequency is controlled by a synchronization signal that is supplied by a VCO input voltage, which decides the switching frequency f_{sw}.

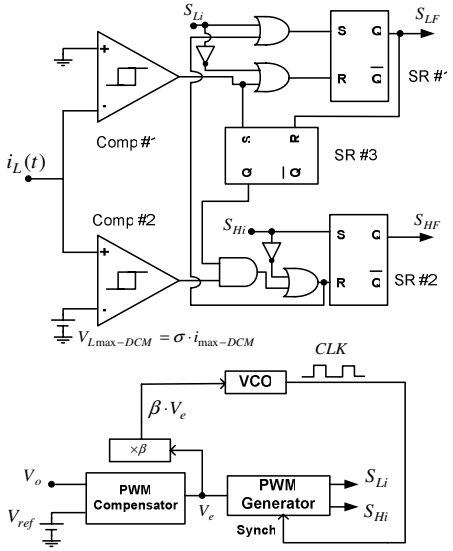


Fig. 5: Proposed Pulse-Sliding Analog Implementation

The VCO input voltage is controlled by voltage signal proportional to the PWM compensator error signal ($\beta \cdot V_e$). Note that $\beta \cdot V_e$ is proportional to the duty-cycle, which starts with a large value at CCM-

DCM transition region and drops quickly as VR goes deep to DCM, which can be used to force higher f_{sw} in the transition mode and lower f_{sw} deep in DCM, providing improved light load efficiency while maintaining low steady-state ripple and good dynamic performance.

In DCM-CCM transition region, V_e value will increase, and hence f_{sw} will increase. This is because of the fact that Comp #2 will turn OFF / reset S_{HF}, earlier than the PWM compensator commanded, to limit the inductor peak current, which will result in a duty cycle that is smaller than what is needed to charge the output capacitor and maintain the output voltage and hence force the PWM compensator/controller to increase V_e to deliver larger duty cycle. Increasing V_e will result in increasing f_{sw} and hence eventually decreasing the ripple below the limit and reaching a steady-state.

V. Compensation Desgn and Dynamic Performance

Good dynamic performance is important to be maintained at all conditions especially if the load has strict dynamic requirements. Since the modes of operations in the presented technique are changed along with f_{sw}, the VR closed loop design should consider these changes. The VR buck power stage has different transfer functions and responses as derived in [3,4]. As shown in Fig. 6, a compensator design for the power stage specifications mentioned in Section III is carefully designed to perform well in CCM and in DCM. Details are omitted because of space limitations.

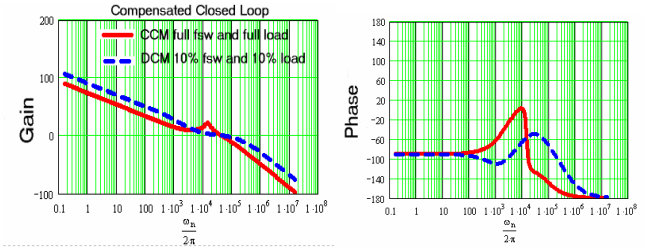


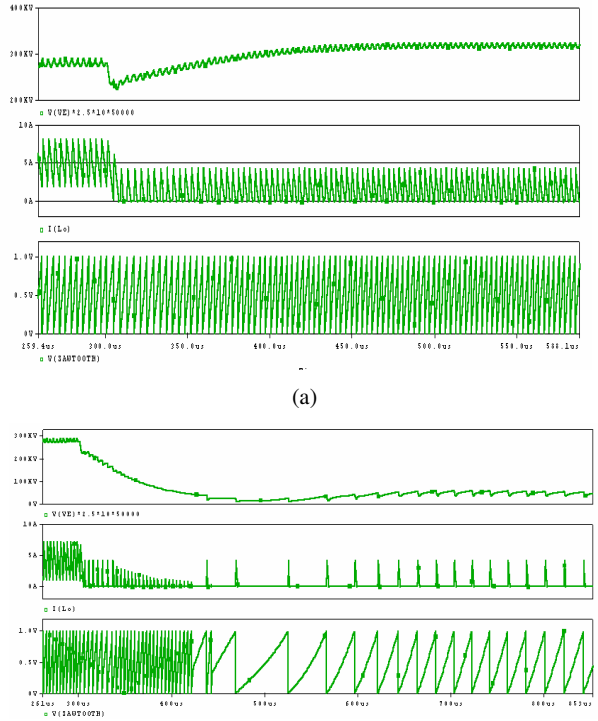
Fig. 6: VR Closed Loop Frequency Response Pode-Plots

VI. Simulation And Experimantal Work

Parts of the efficiency analysis simulation results were presented though out the paper. The presented method implemented by Fig. 5 is circuit simulated using Pspice/Orcad to verify the operation concept, as shown in Fig. 7. In Fig. 7(a), the load switches from high to low (5A to 1.5A) to the edge of the CCM-DCM transition which causes f_{sw} to slightly increase to maintain the ripple below the specified limit. In Fig. 7(b), the load switches from high to very low (4A to 0.2A) far from the edge of the CCM DCM transition (deep into DCM region) which causes f_{sw} to decrease to increase the efficiency while maintaining the specified ripple. The experimental work with the specifications of Section III is in progress and to be reported in the final paper ad future publications with details and discussion.

VII. Conclusion

Analysis and design of VR considering lighter loads efficiency is discussed in this paper. Review of several techniques along with their power loss analysis curves for a design example is presented. Moreover, a load adaptive control scheme with non-linear variable frequency, namely Pulse-Sliding, is presented in this paper to improve VR light load efficiency while maintaining good steady-state and dynamic performances. Concept, analysis, and implementation of the proposed scheme are briefly discussed. The implementation is verified by Pspice/Orcad simulation results. Because of the fact that experimental paper is still in progress at the time of this paper submission and also because of the space limitation, experimental results are left for future publication.



(a)

(b)

Upper Trace: Switching Frequency

Middle Trace: Inductor Current

Lower Trace: PWM Modulation Ramp

Fig. 7: Pspice/Orcad Simulation Results (a) Load Operation from CCM to Edge of DCM, and (b) Load Operation from CCM to Deep DCM

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