ARCHITECTURES FOR ENERGY-AWARE IMPULSE UWB COMMUNICATIONS

Raúl Blázquez, Anantha Chandrakasan

Massachusetts Institute of Technology
38-107, 50 Vassar St., Cambridge, MA 02139, USA
rbf@mit.edu, anantha@mtl.mit.edu

ABSTRACT

Ultra-wideband (UWB) signaling is an emerging technology that promises high data rates at a very low power cost. Due to the complex characteristics of the UWB channel, the signal processing required to achieve high data rates even at low distances is very large. In this paper, the complexity trade-offs associated with three elements of the digital baseband: the correlators bank, the RAKE receiver, and the Viterbi based MLSE equalizer, will be presented for a practical transceiver.

1. INTRODUCTION

Ultra-wideband transmission is currently restricted by the FCC to the band between 3.1 GHz and 10.6 GHz, a maximum equivalent isotropic radiated power (EIRP) spectral density of -41.3 dBm/MHz, and a minimum bandwidth of 500 MHz. The IEEE 802.15.3a standard group is currently developing a high data rate UWB standard for Wireless Personal Area Networks (WPAN). A pulsed UWB transceiver with the FCC spectral mask is being developed. A large percentage of the power dissipation of these transceivers is associated with the signal processing in the digital baseband, making the optimization of this part relevant for the system. This prototype focuses on providing a flexible platform that exposes several knobs to trade off quality of service with signal processing complexity, and therefore, power dissipation; this allows the transceiver to adapt to the channel characteristics.

2. UWB SYSTEM CONSIDERATIONS

We are currently developing a UWB system to operate in the 3.1-10.6 GHz band. The signal is comprised of a sequence of 500 MHz bandwidth pulses that are upconverted to one of 14 channels (sub-bands) in the 3.1-10.6 GHz band. The interval between every two consecutive pulses is T_s=10 ns. Every bit of information is represented in BPSK by only one pulse, achieving a data rate of 100 Mbps. For example, Fig. 1 shows a 500 MHz pulse with a carrier of 5 GHz. This pulse was measured in a discrete testing platform for UWB transceiver that permits to test the receiver algorithms under realistic conditions. This platform is flexible enough to generate different kinds of signals within a bandwidth of 500 MHz, allowing the comparison between different modulation

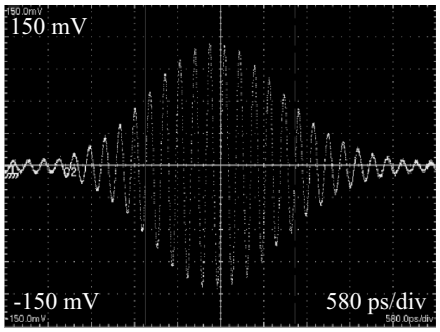

Figure 1. Measured 500 MHz pulse at 5 GHz carrier

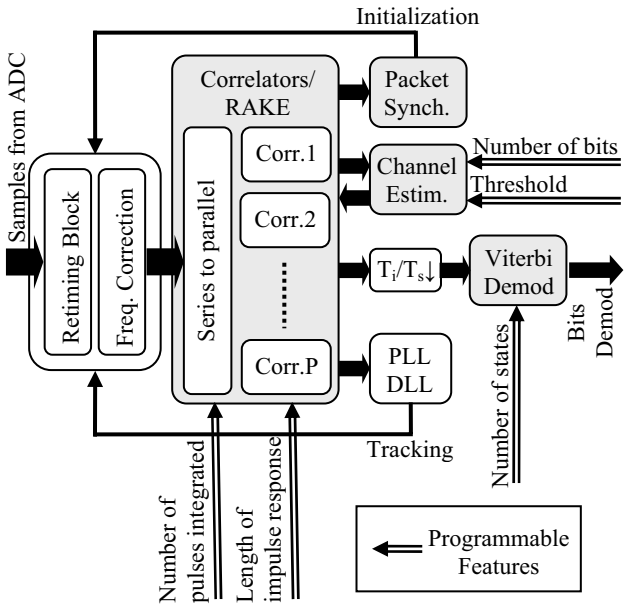

Figure 2. UWB Digital Baseband Algorithms

schemes.

The UWB channel, is impaired by a severe multipath. [1] presents 4 channel models for indoor environments with transmission distances smaller than 10 m. These channels are identified as CM1 (with rms spread delay, $T_{rms,}$, equal to 5.05 ns), CM2($T_{rms,}$=8.03 ns), CM3 ($T_{rms,}$=8.03 ns) and CM4 ($T_{rms,}$=25 ns),

Multipath may be compensated with a RAKE receiver and the inter-symbol interference, which occurs whenever the channel impulse response is longer than the symbol period, counteracted with a Viterbi based MLSE equalizer [2].There is a second impairment of the UWB channel: the presence of in-band interference. The band that UWB signals may use is unprotected and other wireless services already operate within its limits, most notably, 802.11a in the 5 GHz band.

Fig. 2 presents the block diagram of the digital baseband required to demodulate the pulsed UWB signal. This system assumes a direct conversion to baseband architecture in the front-end and in-phase and quadrature components sampled at 500 MSps. In this block diagram, the programmable features that permit to adapt the receiver to the channel characteristics are indicated. Details on the trade-offs associated with the blocks in gray will be considered in this paper. For the rest of the paper, ideal knowledge of the channel impulse response is assumed. It is possible to get arbitrarily close to this assumption during the preamble of the data packet. For the RAKE receiver and the MLSE equalizer, perfect timing synchronization is assumed during the packet payload. This is feasible using both a Delay Locked Loop (DLL) and a Phase Locked Loop (PLL).

3. DIGITAL BASEBAND TRADE-OFFS

This section presents several ways of trading off complexity and, therefore, power dissipation with quality of service in the digital baseband.

3.1. Correlators

The time to achieve packet synchronization is a critical specification of any high data rate wireless system. The length of the preamble must be long enough to guarantee a high probability of achieving signal acquisition. Since a system like 802.11a has a preamble of 20 μs, the same requirement is specified for the UWB transceiver.

The preamble of the data packet is comprised of a sequence of 500 MHz bandwidth pulses at a pulse repetition frequency of 10 MHz. The sign of these pulses is modulated with a 31-bit Gold code. The inter-pulse interval, 100 ns, is larger than the expected impulse response duration, ensuring no ISI corrupts the preamble. Once packet synchronization has been achieved, this permits the estimation of the channel impulse response. The complexity required grows with the signal bandwidth, the duty cycle, and the length of the Gold Code.

Fig 3. shows the block diagram of the correlator bank. It is comprised of P parallel correlators and each of them is time-shared to perform q correlations during the same iteration. These correlators compare the incoming signal with $q \cdot P$ differently delayed templates of a sequence of pulses of 1 sample width whose sign is modulated with the Gold code. If the result of the correlations meets a predefined threshold, T_{h0} , packet synchronization is declared. After the series to parallel block the clock frequency is reduced to $1/P$ of the sampling frequency. P and q are chosen so that $q \cdot P$ equals the number of samples in the inter-pulse interval. The number of pulses used to make a decision about the synchronization, $N_{I,}$ may be chosen independently of the length of the Gold code. $N_{I,}$ controls the Reset signal, that is equal to zero at the beginning of the correlation and to one during the rest of the correlation. The duration of a correlation iteration is

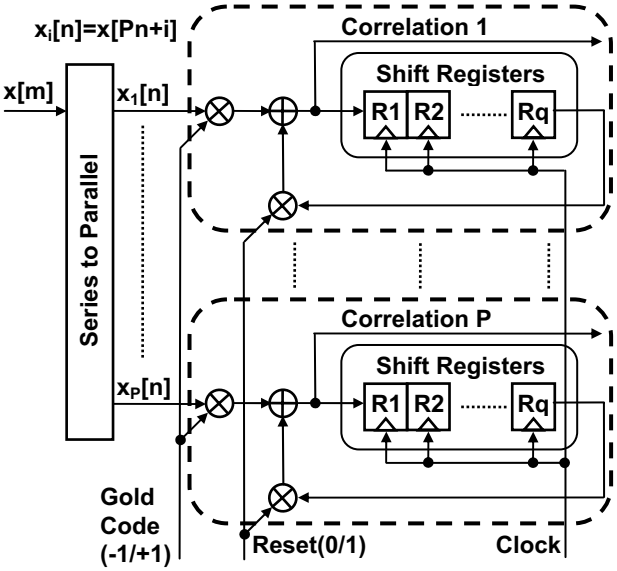

Figure 3. Correlators Architecture

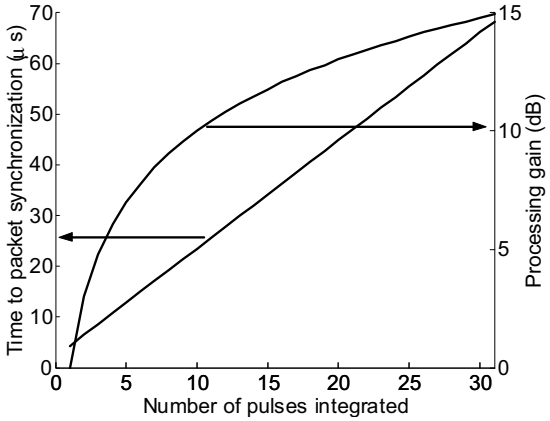

Figure 4. Coarse acquisition trade-off

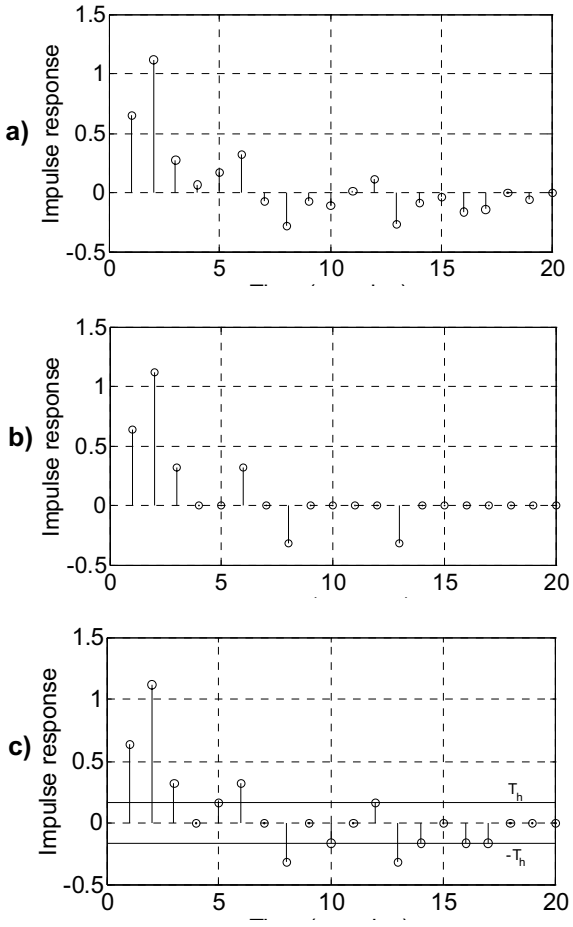

Figure 5. (a) Example of CM1 channel impulse respose (b) As seen with a RAKE of 6 fingers. (c) as seen with the modified RAKE receiver

(N_I+1)·100 ns. The extra 100 ns provides time to compare the correlation results to T_{h0}, and, if packet synchronization is not declared, it slides 100 ns the position of the local templates with respect to the incoming signal.

Fig. 4 was obtained assuming that the probability of detecting the incoming signal when it is synchronized is 0.95, and the probability of declaring detection when this is false is 10^{-5}. It shows that it is possible to reduce the average synchronization time below 20 μs if N_I < 9, although this implies a processing gain of 9 dB over the case where only 1 pulse is used, and 6 dB below the case where the whole Gold code is used. This loss is reasonable for the SNR expected for this application.

The number of operations performed by the correlators is roughly independent of N_I. Moreover, this architecture also provides the estimation of the channel impulse response after packet synchronization has been achieved. Any precision required for this estimation may be obtained by increasing arbitrarily N_I.

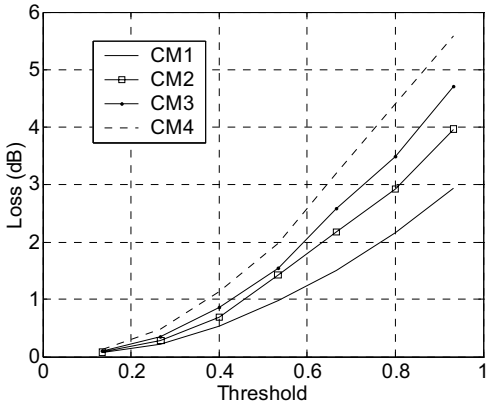

Figure 6. Losses in the modified RAKE receiver as a function of the normalized threshold and the channel model

3.2. RAKE receiver

The channel impulse response is estimated during the packet preamble and estimated with 4 bits precision. This information is used in a RAKE receiver [3] to compensate for the multipath. Instead of having a fixed number of fingers, *F,* this RAKE uses every sample of the channel impulse response that meets a programmable threshold T_h. Either all the samples with the same absolute value are used simultaneously or none at all. For example, Fig.5(a) shows the impulse response of a CM1 channel. Fig 5(b) corresponds to the result of sampling this channel impulse response with 4-bit precision and using a RAKE receiver of 6 fingers. Fig. 5(c) shows the equivalent impulse response if we chose all those impulse responses that go over a threshold equal to T_h = 1 LSB.

By using a threshold, F is a random variable and adapts to the channel impulse response. The block that searches for the most powerful samples in the channel impulse response, required in the RAKE receiver, is replaced by the comparison of its samples to the threshold T_h.

Fig. 6. shows the losses of this RAKE receiver as a function of the normalized threshold and the channel model with respect to the perfect RAKE receiver. This figure was obtained assuming perfect synchronization and a Viterbi based MLSE equalizer of 16 states after the RAKE receiver. Since a decrease of T_h implies a larger F, Fig. 6 shows that signal processing complexity may be traded off with quality of service.

3.3. MLSE equalizer

The Viterbi based MLSE equalizer is used in this architecture to compensate for the inter-symbol interference that occurs when the channel impulse response is longer than the time between two consecutive

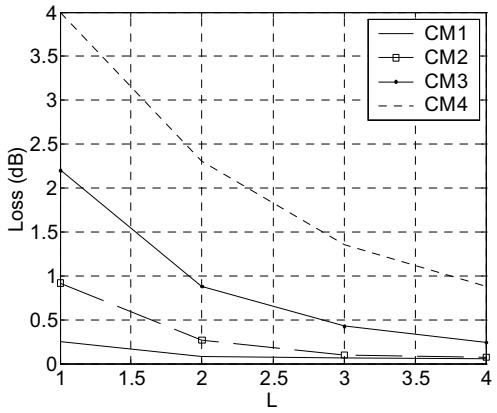

Figure 7. Losses associated with the parameter L in the Viterbi demodulator

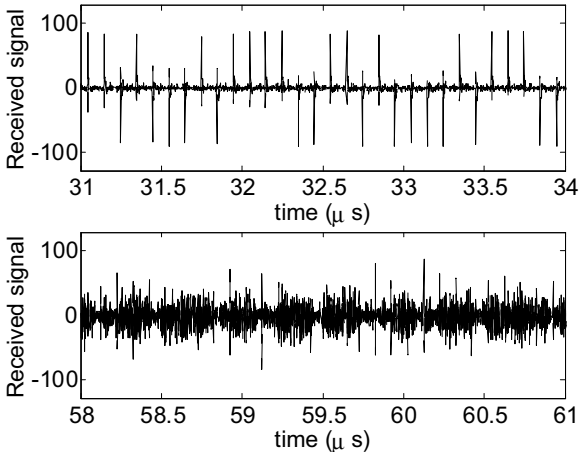

Figure 8. Part of the preamble of a data packet as measured in the discrete prototype, without (above) and with an interference(below).

pulses. It is possible to obtain the number of states in a MLSE equalizer depending on the length of the impulse response of the channel, L_{mp} [2]. The number of states required for a BPSK signal in the MLSE equalizer is 2^L with:

$$L = \left\lfloor \frac{L_{mp}}{T_s} \right\rfloor \qquad (1)$$

The MLSE equalizer implemented will be able to cope with a predefined maximum channel impulse response. It is possible to downscale the MLSE equalizer if the length of the impulse response does not require the use of the entire number of states. Since the complexity of the MLSE equalizer is exponential with parameter L [4] this will lead to important power savings.

Fig. 7 shows the losses associated with the MLSE equalizer as a function of parameter L. This figure assumes a RAKE receiver with a threshold T_h equal to 1 LSB. For both channel models CM1 and CM2, even without using a MLSE equalizer (or using one of 2 states), a maximum loss of 1 dB is obtained. Channel model CM3 will provide a satisfactory performance with a MLSE equalizer of 4 states. Only CM4 requires higher complexity than this.

4. A ROBUSTNESS TEST

This baseband processor was tested using a the UWB discrete platform mentioned in section 2. Fig. 8 shows an example of a part of the preamble of the data packet as measured in this discrete prototype using an FCC compliant signal centered at 5 GHz in a wireless link without interference and affected by an interference with an SIR = -11 dB in the preamble. The receiver achieved packet synchronization in presence of the interferer in less than 20 μs using N_L = 9 pulses, the channel impulse response was measured to be below the inter-pulse interval of the payload, and a whole data packet of 10000 bits was perfectly demodulated without using the Viterbi based MLSE equalizer.

5. CONCLUSIONS

In this paper, the architecture for a digital baseband processor has been presented. The different blocks of this architecture expose several knobs that permit to trade off quality of service with time to achieve packet synchronization, signal processing complexity and power dissipation. The correlators provide not only enough information to achieve fast packet synchronization, but also the whole channel impulse response estimation. This information and the flexibility of the digital baseband permits to adapt the receiver power dissipation to the channel characteristics and the desired quality of service.

ACKNOWLEDGMENTS

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