MULTIPLIERLESS REALIZATION OF BANDPASS AND BANDSTOP DIGITAL FILTERS TRANSFORMED FROM ALL-POLE LOWPASS FILTERS

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ABSTRACT

In our earlier investigations on developing multiplierless structures for digital recursive filters, we have shown that utilizing low-sensitivity structures and appropriate transformations it is possible to generate multiplierless implementations of bandpass and bandstop filters. The schemes are quite attractive when we allow marginal deviations in the specifications, or start with a design of marginally stricter specifications than the desired specification without any increase in the filter order leading to quite low requirements of nonzero bits. In this paper we present results for the structure that employs the low-sensitivity characteristics of the all-pole type of structure for developing multiplierless implementations of bandpass and bandstop digital recursive filters transformed from all-pole lowpass filters.

1. INTRODUCTION

In multiplierless implementations of digital filters, the minimum number of signed powers of two (MNSPT) or canonic signed digits (CSD) representations of binary digits are extensively used for representing the multiplier coefficient values. An MNSPT representation of a coefficient value is given by $\sum_i a_i 2^{-t_i}$, where each a_i is either 1 or –1 and t_i is a positive or negative integer and the multiplication can be performed with the aid of bit shifts and adds (in this paper, adds will mean to include adds and/or subtracts).

For instance, 1.93359375 can be realized as $2–2^{-4}–2^{-8}$. In this case, the multiplication is achieved not by a nine-bit multiplier, but with aid of three bit shifts and two subtracts.

One major approach for multiplierless implementations comprises of that of optimization [11, 12], i.e., searching for the coefficients such that they can be implemented in MNSPT forms and the given criteria are still met. Optimization methods are used to find the optimal transfer functions under the given constraints with the filter design being basically a problem of approximation due to the tolerances in specifications. In general, the methods of optimizations are considered to be quite satisfactory. However, one may not assure or guarantee that the optimal solution will always be found under the given constraints. The solution can be unsatisfactory, for example, in terms of the filter order, the given wordlength of the multipliers, or the specified number of shifts and adds (in the case of the multiplierless implementation), or some combination of them. Under such conditions, some parameters or characteristics of the filter will have to be relaxed to obtain an acceptable design for use in the intended system.

In the case of IIR filters, the structures such as a sum of two allpass filters, including attractive lattice wave digital (LWD) filters, coupled with optimization methods have shown to yield good results for multiplierless implementations [6, 7, 11, 12]. These sums of allpass filters are characterized by the attractive property that there exist structures with the number of required multipliers being equal to the filter order, thereby decreasing the number of multipliers compared with conventional realization forms.

Another interesting approach is the one that stems from designing an odd-order elliptic minimal Q-factor analog filter (EMQF) that has some special properties. Using the bilinear transformation these filters can be implemented as a sum of two allpass filters [6, 7] along with an expanded design parameters space as the passband (stopband) tolerances, the edges, and the filter order.

The authors of this paper have been investigating the multiplierless realization of the recursive digital filters [1, 2, 8] based on the certain observations.

Firstly, it was seen that in certain cases of the low-sensitivity structures [3, 4], the modified coefficients are quite low, those will require fewer number of nonzero bits to represent them in MNSPT forms; this results in fewer number of operations in terms of shifts and adds. So, these classes of structure became the candidates for further investigation.

Secondly, it was also observed that the requirement of nonzero bits can be reduced further if instead of designing exactly to the given specification, one starts by designing with a stricter specification without any increase in the order of the filter, followed by quantization to the level such that the initial specifications are met [1, 2, 8]. As an illustration, if our goal passband tolerance is 0.5 dB, we may start with a design of 0.3 dB (without any increase of the order of the filter) and then quantize the coefficients such that the goal passband of 0.5 dB or less is achieved.

Thirdly, in the case of bandpass filters (BPFs) or bandstop filters (BSFs), it is always advantageous to use appropriate second-order substitution block to replace the unit delay element, for transforming a prototype lowpass filter (LPF) [2, 4]. In this case, we gain from two advantages that of firstly the reduced number of multiplier requirement and secondly the inherent low sensitivity of the α–multipliers (explained in the next section) in the substitution blocks [2, 4]. A second-order LPF section is realized as a fourth-order section for transforming it to a BPF/BSF section.

In this paper, we show that it is feasible to transform a all-pole LPF to a multiplierless BPF/BSF in such a manner that the requirements of nonzero bits are equally attractive compared to our earlier results.

2. THE STRUCTURES FOR REALIZATION

The fourth-order structure of the BPF/BSF that is being transformed from a second-order LPF with transfer function

$$H(z) = 1/(1 + a_1 z^{-1} + a_2 z^{-2}) \qquad (1)$$

is depicted in Fig 1.

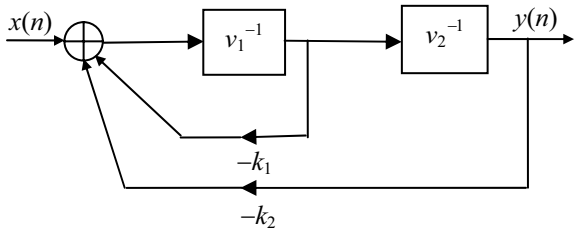

Fig. 1. Modified fourth-order section.

The transformation blocks v_i^{-1}, i=1, 2, are shown in Fig. 2. As will be explained in the following paragraphs, these two blocks are not interchangeable and are specific to the second-order section of the LPF being transformed to a fourth-order section, as the modified coefficients are contained in them.

Here, k_1 and k_2 are of the form $\sum_i p_i 2^{t_i}$, where each p_i is either 1 or −1 and each t_i is an integer. These multipliers can be realized by using a few bit shifts and adds. Normally, the maximum of three bits for k_1 and two bits for k_2 are sufficient to reduce the sensitivity below that of the majority of other structures [3]. The values of k_1 and k_2 are chosen depending on the radius and angle of the pole pair of the second-order LPF as given by (1). The corresponding pole pair is located at $z = re^{\pm j\theta}$ with $a_1 = -2r\cos\theta$ and $a_2 = r^2$.

The expressions for v_i^{-1}, i=1, 2, are given by

$$v_i^{-1} = \frac{k_t(z^{-2} - \alpha z^{-1})}{1 - \alpha(1 - k_t a_{im})z^{-1} - k_t a_{im} z^{-2}}. \qquad (2)$$

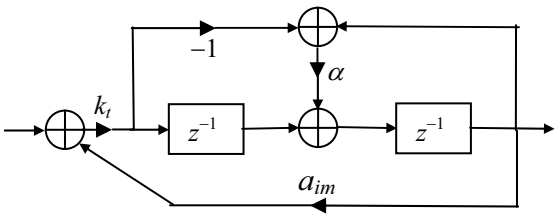

Fig. 2. Transformation block v_i^{-1}.

In (2), k_t is equal to −1 in the case of BPFs, and is equal to +1 in the case of BSFs. Also, a_{1m} and a_{2m} are the modified multiplier coefficients and are given by

$a_{1m} = (2k_1 - a_1 + x)/2$ and $a_{2m} = -(a_1 + x)/2$ for $0 < \theta < \pi/2$ (3)

and

$a_{1m} = (2k_1 - a_1 - x)/2$ and $a_{2m} = (-a_1 + x)/2$ for $\pi/2 < \theta < \pi$. (4)

Here,

(i) $x = (a_1^2 - 4a_2 + 4k_2)^{1/2}$.

(ii) k_1 is a few bit approximation closest to
$(a_1 - x)/2$ for $0 < \theta < \pi/2$, and
$(a_1 + x)/2$ for $\pi/2 < \theta < \pi$.

(iii) k_2 is a few bit approximation closest to a_2 with k_2 being chosen before k_1 ensuring that x remains real [3].

The α–multiplier is given by (as in[5])

$$\alpha = \cos[(\omega_2 + \omega_1)/2]/\cos[(\omega_2 - \omega_1)/2] = \cos\omega_0, \qquad (5)$$

where $\omega_0, \omega_1, \omega_2$, and ω_s are the center frequency, and the lower and upper passband edges, and the sampling frequency, respectively. This relation is valid only for the case of BPF's with the passband bandwidth $(\omega_2 - \omega_1)$ being equal to that of the prototype LPF, and in the case of BSF's with $(\omega_2 - \omega_1)$ (i.e., the region including the tran-

sition bands and the stopband of the BSF) equaling ($\omega_s / 2$ – the bandwidth of the LPF) [4, 5].

It is quite obvious that when implementing this fourth-order section, we will need four multipliers including the two α–multipliers, whereas a conventional implementation by a cascade of the two second-order sections (as obtained by the factorization after the transformation to a BPF/BSF) would have required total of six multipliers (three multipliers per second-order section) [2, 4].

3. RESULTS AND DISCUSSIONS

Realizations of quite a few bandpass and bandstop filters transformed from all-pole filters were experimented as described in the earlier section. The all-pole filters were designed according to the very simple design scheme described in [9, 10]. For most of the cases one bit is sufficient for each k_1 and k_2.

Tables 1 and 2 illustrate the results for the implementation for one bandpass filter and one bandstop filter. In both cases, eighth-order all-pole LPFs were used for transformation to 16th-order BPF/BSF. The second-order sections of the all-pole LPF were transformed into fourth-order sections as depicted in Figures 1 and 2. Quantization effects at various levels of fixed point arithmetic (excluding sign bits) were studied for feasibility of multiplierless realization as described subsequently.

Firstly, the filters were realized in the unmodified manner as a cascade of fourth-order sections, where the unit delay elements of the second-order sections of the all-pole LPF as in (1) is replaced by the conventional second-order substitution block [2, 4] as expressed below.

$$z^{-1} \rightarrow k_t (z^{-2} - \alpha z^{-1}) / (1 - \alpha z^{-1}) \qquad (6)$$

As mentioned earlier, k_t is equal to –1 in the case of BPFs, and is equal to +1 in the case of BSFs.

Quantization of the multipliers were carried out to determine the level of quantization at which the specification can be met followed by the representation in the MNSPT form that gives the requirement of nonzero bits (illustration of this aspect is shown in the note of both Tables 1 and 2).

In the next phase the realization of the sections were carried out in the modified manner and quantization effects at some levels (some of them also show the degradation of the passband tolerances; no significant degradation in stopband tolerances are observed, and hence not mentioned in the tables, as expected within the range of observation) along with the requirement of nonzero bits are made as earlier and are shown.

This is followed by designing another prototype all-pole LPF of the same order, but with the stricter passband tolerance and transforming this LPF to the modified form, as in the earlier phase; quantization was made so that the initial desired specifications are met.

Table 1. Requirement of nonzero bits for the example bandpass filter.

Bandpass filter (16th-order) passband edges: 0.3π, 0.4π stopband edges: 0.275π, 0.432π passband ripple: 0.5 dB; stopband attenuation: 50 dB	
Number of nonzero bits for 16 multipliers	Passband tolerances obtained
(a) 85	0.4955 dB designed with initial specification
(b) 83	0.514 dB ……”……
(c) 80	0.5325 dB …..”……..
(d) 53	0.33 dB designed with revised specification of passband ripple of 0.2 dB of the prototype LPF.
Note: Cascade realization of unmodified 4th-order sections needs 22-bit multipliers for coefficients and 16-bit multipliers for α–multipliers (equivalent to a total of 115 nonzero bits in MNSPT form representation)	

Table 2. Requirement of nonzero bits for the example bandstop filter.

Bandstop filter (16th-order) passband edges: 0.05π, 0.85π stopband edges: 0.081π, 0.765π passband ripple: 0.5 dB; stopband attenuation: 50 dB	
Number of nonzero bits for 16 multipliers	Passband tolerances obtained
(a) 95	0.499 dB designed with initial specification
(b) 91	0.5007 dB ……”……
(c) 88	0.501 dB …..”……..
(d) 82	0.506 dB ……”…….
(e) 53	0.448 dB designed with revised specification of passband ripple of 0.2 dB of the prototype LPF.
Note: Cascade realization of unmodified 4th-order sections needs 17-bit multipliers coefficients and 15-bit multipliers for α–multipliers (equivalent to a total of 97 nonzero bits in MNSPT form representation)	

From the results of the Tables 1 and 2, we note that on the average about 3.5 nonzero bits per multiplier is sufficient to realize the BPF/BSF in a multiplierless manner. This result is very much similar to our earlier investigations [1, 2, 8].

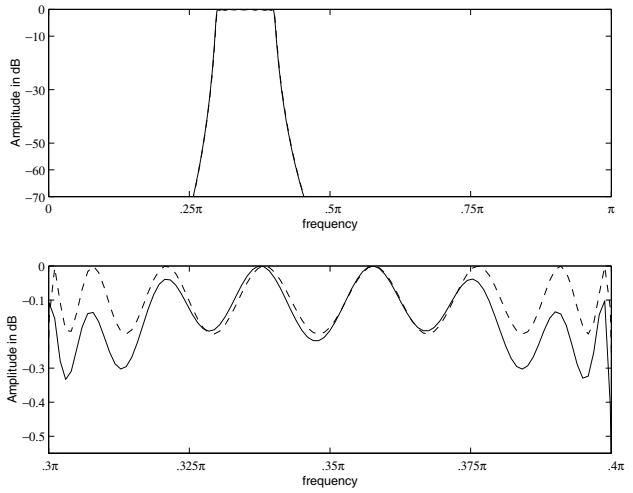

Fig. 3. Amplitude responses for the infinite-precision BPF filter with stricter criteria (dashed line) and for the filter with fifty-three nonzero bits (solid line).

Further, it was also seen that by allowing marginal deviations in the band edges (by reducing the number of nonzero bits for α–multipliers only), an additional reduction in the number of nonzero bits can be achieved. For example, in the case of the BPF, 45 nonzero bits (a reduction of one bit in each of the eight α–multipliers leading to less than three nonzero bits per multiplier on the average) leads to the filter with the passband edges being located at $\{0.2965\pi, 0.3971\pi\}$. The corresponding stopband edges are located at $\{0.2723\pi, 0.4278\pi\}$.

Similarly, the use of 37 nonzero bits (a reduction of two bits in each of the eight α–multipliers again leading to less than 2.5 nonzero bits per multiplier on the average) for the multipliers for the BSF leads to a filter with the passband and the stopband edges being located at $\{0.05092\pi, 0.8497\pi\}$ and at $\{0.0813\pi, 0.766\pi\}$, respectively. Such shift in band edges may be considered insignificant for most of practical applications.

4. CONCLUSIONS

In this paper, we have shown that the multiplierless implementation of BPFs and BSFs utilizing transformation structures suitable for transforming all-pole LPFs, is a feasible and attractive proposition. Considering the acceptance of a marginally small deviation in the passband and stopband tolerance specifications compared to the initial infinite-precision design, the method becomes quite attractive for implementing IIR BPFs and BSFs in the multiplierless manner. Our analysis indicates that utilizing the approach outlined multiplierless realizations can be achieved by using less than four nonzero bits per multiplier on the average without any increase in the filter order. Future work is devoted to applying optimization techniques to further reducing the number of nonzero bits.

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