PHASERECONSTRUCTION RECEIVER WITH COMPENSATION OF NONLINEARITIES

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ABSTRACT

A number of modern wireless systems use modulation schemes like CPFSK, GMSK and DPSK, where the information to be transmitted is exclusively coded in the phase change of the RF-signal. Thus a phase reconstruction receiver can be used, which is based on a simple limiter for digitization. With respect to implementation costs and power consumption this is a very attractive receiver concept. However, due to non-idealities of the RF-front end, the receiver signal can deviate from the ideal PSK-constellation. This can result in performance losses compared to a linear receiver with a high resolution A/D-converter. For the more sophisticated modulation schemes like MPSK, which will be extensively used for high-data rate systems, these performance losses can be severe. Thus in this contribution a digital compensation technique for a phase reconstruction receiver will be proposed, which reduces the nonlinear distortion introduced by the limiter. Using this method an excellent performance can be obtained with a phase reconstruction receiver also for the more sophisticated modulation schemes.

1. INTRODUCTION

Modern short-range wireless systems, e.g. systems according to the Bluetooth-, HomeRF- or DECT-standard [1, 2], use CPFSK as modulation scheme. Whereas classical receivers for CPFSK-modulated signals are based on an FM-demodulator with a limiter discriminator [3], due to the advancement of digital signal processing, architectures using a low intermediate frequency (IF) became more and more popular in the last years [3-6]. In the respective implementations the analogue IF-signal must be digitized by additional A/D-converters. FM demodulation and signal detection can be performed then by methods of digital signal processing [4]. The performance improvements thus obtained, must be paid for by higher implementation costs and higher power consumption for the A/D-converters, however.

Implementation costs and power consumption can be drastically reduced by replacing the A/D-converters by simple limiters. It has been shown, that for simple 2-ary modulation schemes like GFSK no severe performance losses must be taken into account due to the limiter [7].

The wireless communication standards mentioned above have been enhanced with respect to higher data rate capabilities recently [8]. For the higher data rates M-ary modulation schemes such as DPSK are proposed, where for the signal beam-forming a root raised cosine filter is preferably used. Examples taken from the Bluetooth-specification are DQPSK for 2 Mbit/s and 8-DPSK for 3 Mbit/s data rates. Note however that for the more sophisticated modulation schemes the transmit signal does not have a constant envelope anymore.

A key characteristic of these enhancements is that a switching from one modulation scheme to the other must be possible. Thus the receiver in the respective terminal must be able to process the 2-ary and the M-ary modulation schemes as well. With respect to cost and power consumption requirements it is desirable to use again the simple receiver concept with the limiter. For Enhanced data rate Bluetooth systems this can be achieved by modifying the simple CPFSK-receiver to a combined CPFSK/PSK-architecture. A straightforward extension of the conventional limiter receiver to M-ary modulation schemes however results in severe performance losses compared to a linear receiver.

In order to avoid these performance losses, the limiter input has to be mapped to the M-PSK-constellation. In [9] it has been shown, that this mapping can be performed by using a matched filter for channel-selection. If an RRC-filter is used on the transmit side the respective matched filter in the receiver must have also an RRC-characteristic. In this case the IQ-constellation at the synchronization points correspond to the MPSK-constellation, the digitization by the 1 Bit A/D-converters does not add distortion to the signal. However, since the filter is implemented in the analog domain, deviations from the ideal RRC-characteristic due to tolerances still must be taken into account. Furthermore, due to the recursive structure normally used for this filter, some group delay distortion is introduced. Due to these non-idealities the input signal of the limiter will still deviate to some extent from the ideal M-PSK-constellation. Thus the limiter will add some non-linear distortion to the received signal resulting in respective performance degradations.

Since these performance degradation in most cases cannot be tolerated, nowadays receivers for M-ary modulation schemes use higher resolution A/D-converters. A performance close to that of an ideal receiver can be thus obtained for a sufficient resolution of the ADCs (e.g. 10 Bits) with the drawback of higher costs and power consumption however.

2. PHASE RECONSTRUCTION RECEIVER

Fig. 1 shows the block-diagram of the phase reconstruction receiver. The RF-front end, not shown in fig. 1, performs down-conversion of the received RF-signal to a low intermediate frequency. For Bluetooth typical values for the low IF are 1 or 2 MHz [4, 5]. In the next step the complex IF-signal is band limited by the channel selection filter. Then the limiters, operating with an over-sampling ratio of OSR with respect to the symbol rate, generate binary signals from the filtered I- and Q-components. These binary signals still contain the information about the phase $\Phi(t)$ of the received signal in their zero transitions. The phase reconstruction module behind the limiters reconstructs the instantaneous phase $\Phi(t)$ of the received IF signal by methods of digital signal processing. The input to this module are the time instants t_j of zero-crossings which are used for determination of the respective instantaneous phase values $\Phi(t_j)$.

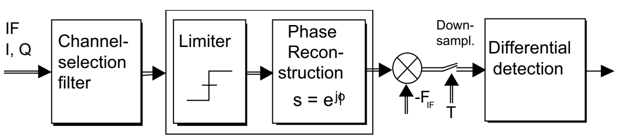

Fig. 1. Receiver for CPFSK-modulated signals with hard-limiting of the IF-signal and a DSP-module for phase reconstruction.

This can be done e.g. for CPFSK by observing that the instantaneous phase of the inphase and quadrature components increases by π with each zero-crossing if the intermediate frequency is chosen appropriately. If the instantaneous phase is band-limited with cut-off frequency Ω the instantaneous phase $\Phi(t)$ is obtained by following iterative reconstruction algorithm [10].

$$\Phi_n(t) = \Phi_{n-1}(t) + \lambda \cdot \sum_{j=-\infty}^{\infty} \left[\Phi(t_j) - \Phi_{n-1}(t_j)\right] \cdot \frac{\Omega}{\pi} \cdot \operatorname{sinc} \frac{\Omega}{\pi}(t - t_j)$$

Here, λ denotes a relaxation parameter and $\operatorname{sinc}(u)=\sin(\pi u)/(\pi u)$. Since

$$h(t) = \frac{\Omega}{\pi} \cdot \sin c \frac{\Omega}{\pi}(t - t_j)$$

is the impulse response of an ideal low-pass filter with cut-off frequency Ω. Fig. 2 shows the block diagram of this iterative phase reconstruction algorithm. The phase reconstruction requires that the sampling rate of the limiters is considerably higher than the intermediate frequency.

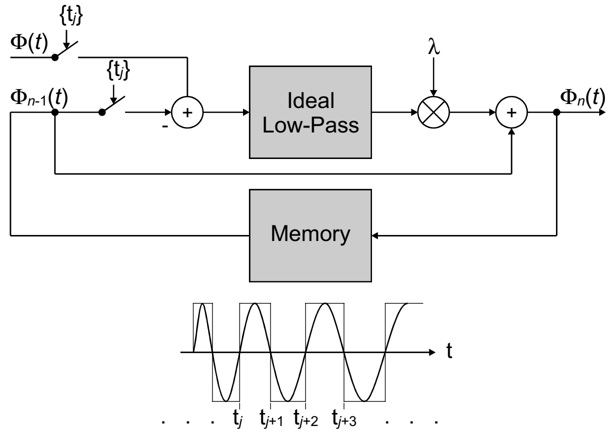

Fig. 2. Block diagram of the phase reconstruction module.

A reasonable value for the over-sampling ratio is e.g. 52 or 104. The input signal of the limiter can be described by:

$$\begin{aligned} s_{IF}(t) &= A(t) \cdot e^{j2\pi f_{IF} t} \\ &= \left|A(t)\right| \cdot e^{j\varphi_A(t)} \cdot e^{j2\pi f_{IF} t} \end{aligned}$$

The information about the signal amplitude $|A(t)|$ gets lost by the limiter operation. The output signal with perfect phase reconstruction is thus given by:

$$\begin{aligned} s_{IFP}(t) &= e^{j\left[2\pi f_{IF} t + \varphi_A(t)\right]} \\ &= e^{j\Phi(t)} \end{aligned}$$

The digital mixer down-converts the signal $s_{IFP}(t)$ to base-band then, so that sample rate reduction to the symbol rate and detection can be performed.

In order to limit the bandwidth of the transmit signal for M-ary modulation schemes, an additional low-pass filtering is performed in the transmitter. The equivalent low-pass signal v(t) is thus given by:

$$v(t) = \sum_k S_k\, p(t - kT)$$

where T is the symbol duration, and p(t) is the impulse response of the low-pass filter. S_K is the information bearing constant amplitude signal. For Enhanced data rate Bluetooth systems a root raised cosine filter with impulse response p(t) is specified and T has a value of T=1µs. The respective shape of the frequency spectrum is given by:

$$|P(f)| = \begin{cases} 1 & 0 \le |f| \le \frac{1-\beta}{2T} \\ \sqrt{\frac{1}{2}\left(1 - \sin\left(\frac{\pi(2fT-1)}{2\beta}\right)\right)} & \frac{1-\beta}{2T} \le |f| \le \frac{1+\beta}{2T} \\ 0 & elsewhere \end{cases} \qquad (1)$$

The roll-off-factor β determines together with T the required bandwidth.

Behind the RF-mixer the output of the transmitter is a band-pass signal and can be described as follows:

$$s(t) = \mathrm{Re}\left\lfloor v(t)e^{j2\pi f_c t} \right\rfloor,$$

where f_c is the RF carrier frequency. On the transmit path this signal is corrupted by cochannel- and adjacent channel interferers and other noise sources. In the receiver it is down-converted to the low IF and filtered by the channel-selection filter.

Due to the RRC pulse shaping the information about the data symbols is not only contained in the phase anymore but also in the amplitude of the received signal. Thus even if the phase of the signal at the limiter can be completely reconstructed, performance losses must be taken into account.

In order to avoid these performance losses, the limiter input signal has to be mapped to the M-PSK-constellation. This can be achieved by a channel-selection filter with RRC-transfer characteristic. In this case it also operates as a matched filter for the data. Furthermore the signal is free of intersymbol interference (ISI) and the data symbols correspond to the M-PSK-constellation at the synchronization time instants. When digitizing the respective I- and Q-components by limiters a perfect reconstruction according to the PSK-constellation is possible since at the synchronization time instants the signal amplitude is always $\sqrt{E_{sym}}$ assuming perfect synchronization, with E_{sym} the energy of a symbol. Thus the information is only contained in the phase changes of the limiter input and can be perfectly reconstructed as already described. If the pre-filter is closely matched to the RRC-characteristic a limiter receiver with phase reconstruction shows the same performance as a receiver with high-resolution A/D-converters.

Thus the challenge arises to design an analogue pre-filter with a good match to the RRC-characteristic and which only introduces minor group delay distortion. In [9] it has been shown, that good performance results can be obtained by using a filter with butterworth characteristic. However, since the filter is implemented in the analog domain, deviations of the filter characteristic due to tolerances must be taken into account. If these tolerances increase above a certain limit, again severe performance losses can occur. Fig. 3 shows the constellation diagram for an 8-DPSK signal, where the channel-selection filter has been implemented by a filter with butterworth characteristic. The corner frequency was chosen to f_c=500kHz, which was 10% below the optimum value. The constellation points are degenerated to a cloud around the desired values. Due to the non-ideal pre-filter the limiter introduces non-linear distortion, resulting in performance losses of more than 1dB for this example. In order to reduce these errors a novel compensation method for these non-linearities will be proposed in the next chapter. The improvement for the I/Q-constellation is already shown by the right diagram in fig. 3.

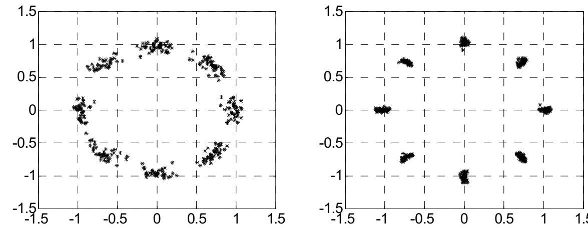

Fig. 3. Constellation diagrams for a an 8-DPSK-receiver with perfect synchronization, base-band I/Q-constellation with limiter (left diagram), respective I/Q-constellation improved by error compensation (right diagram).

3. ERROR ESTIMATION AND COMPENSATION OF NON-LINEARITIES

The mentioned performance losses can be reduced by digital estimation and compensation of the errors. These errors are caused by the nonlinear mapping of the limiter if the input does not exactly correspond to the M-PSK-constellation. Furthermore the limiter receiver is more sensitive with respect to synchronization errors.

The respective block diagram of the improved receiver is shown in Fig. 4. In a first step the IF-signal is processed by the receive path as already described in the previous sections, with pre-filtering, digitization by the limiters, conversion to base-band and post-filtering for suppression of the harmonic distortion. Furthermore, synchronization and down-sampling is performed. For the linear receiver the received symbols $s_R(kT)$ would correspond to the M points of the M-PSK constellation. Due to the limiter and other non-idealities the symbols of the real signal however deviate from the ideal values s(kT) by an error e(kT). Thus the received signal can be described by

$$s_R(kT) = s(kT) - e(kT).$$

These values $s_R(kT)$ are used as input for the error estimator, which maps them to the respective closest values of the M-PSK-constellation. Using these values as input, the error estimator models the signal processing of the transmitter and the receiver for the ideal and for the non-ideal case. The ideal configuration just delays the symbols by a value T_1 (see fig. 4). Thus the difference between both output signals is the estimated error signal $e_e(kT)$ caused by non-idealities of the real configuration. The main sources for this non-ideal behaviour are the distortion introduced by the limiter and the deviation of the transfer function of the pre-filter from the ideal RRC-characteristic.

This estimated error signal is now added to the delayed and decimated receiver signal. Thus a new signal $s_{co}(kT)$ is obtained, which is approximately equal to the delayed signal of the linear receiver. This is shown by the following relationships:

$$\begin{aligned} s_{co}(kT) &= s_R(kT - T_D) + e_e(kT) \\ &= s(kT - T_D) - e(kT - T_D) + e_e(kT) \\ &\cong s(kT - T_D). \end{aligned}$$

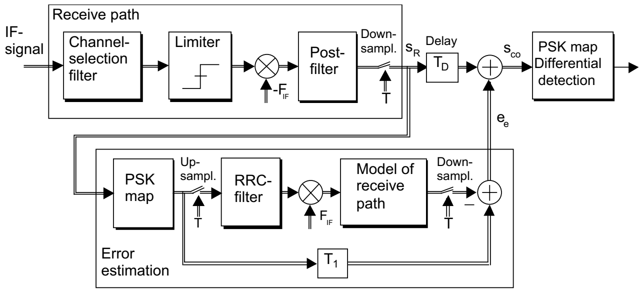

Fig. 4. Limiter receiver with digital estimation of non-linearity errors and compensation.

The compensated signal $s_{co}(kT)$ is used for the final detection. The signal processing in the error estimation block can be efficiently implemented e.g. by using "table-look-up techniques". The method can be also made adaptive so that the effects of varying transmission paths can be compensated.

Methods which show a certain similarity to the proposed error compensation technique are described in [12] for the suppression of distortion generated on the RF-link. They use a digital filter which determines a correction signal based on old decisions. The method proposed in this paper, however, uses a non-linear mapping for the compensation of the limiter non-linearities.

Simulations confirmed the improvements which can be obtained by the proposed estimation and compensation method. This was verified for an AWGN-channel and for other noise sources like co-channel and adjacent channel interferers. The results for AWGN- channel and an non-ideal pre-filter are shown in fig. 5. The performance losses of more than 1 dB due to the imperfect RRC-filter are nearly compensated for by the proposed method.

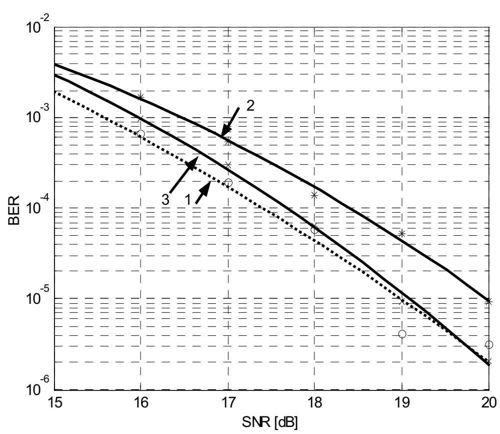

Fig. 5. Signal to noise ratio versus bit error rate for the 8-DPSK-limiter receiver with phase-reconstruction, optimal RRC-pre-filter, f_c=540kHz (curve 1), RRC-pre-filter, f_c=500kHz (curve 2), RRC-pre-filter and error-compensation, f_c=500kHz (curve 3).

4. SUMMARY

In this paper we have described the optimization of a combined CPFSK/PSK-receiver based on a phase reconstruction structure. This type of receiver can be used for Bluetooth enhanced data rate systems. The respective modulation schemes used are DQPSK and 8-DPSK in addition to GFSK. It has been shown that for all modulation schemes a limiter receiver with phase reconstruction can be used. Performance losses which normally have to be taken into account when using a limiter receiver for the higher order modulation schemes, can be nearly compensated for by a novel error estimation and cancellation algorithm described in this paper. The method can be completely implemented in the DSP-part of the receiver. The improvements thus obtainable had been verified by simulation results.

Applying the proposed architecture the limiter receiver shows approximately the performance of a receiver with high-resolution A/D-converters.

5. REFERENCES

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