DIGITAL SIGNAL PROCESSING IN CONTINUOUS TIME: A POSSIBILITY FOR AVOIDING ALIASING AND REDUCING QUANTIZATION ERROR

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ABSTRACT

The operation of digital signal processors in continuous time is discussed. It is shown that the main advantages of digital arithmetic can be maintained in such operation, while aliasing of the signal and the quantization error is avoided altogether. Continuous-time operation makes possible a smaller number of bits for a given signal-to-quantization error ratio. Simulation results are presented.

1. INTRODUCTION

Consider a quantizer with analog input and output, as in Fig. 1(a). For simplicity, we will assume that the input $x(t)$ is sinusoidal, with frequency f. The output $w(t)$ will thus be periodic, and its spectrum will contain components only at $\pm mf$, m integer, as shown in Fig. 1(d); only odd harmonics are found if the quantizer characteristic is symmetric around the origin. In conventional digital signal processing, a sampling operation at a frequency $f_s > 2f$ precedes quantization, as shown in Fig. 1(b). For the purposes of calculating the output, the two operations can be interchanged as shown in Fig. 1(c) without altering the result. In the latter figure it is apparent that, even though the input is properly band-limited, the output of the quantizer is not, due to the many harmonics introduced by the nonlinearity of the latter. Due to the subsequent sampling, these harmonics are aliased to frequencies $\pm pf_s \pm mf$, p, m integers. Assuming that f_s / f is a rational number, the resulting spectrum is discrete, with components falling in-band, as shown in Fig. 1(e). This so-called "quantization noise" is thus equivalent to aliased harmonic distortion. If a bandwidth approximately equal to $f_s / 2$ is considered, the total in-band quantization error power turns out to be approximately equal to that at the output of the quantizer, and for 2^n quantization levels it is given by the classical result of $-(1.76 + 6.02n)$ dB relative to the rms value of the sinusoidal input signal.

The above quantization error can be contrasted to the case of a quantizer without sampling in Fig. 1(a). The total power of the harmonics at the output of the latter, taken over the extremely wide band in which they are found, is the same as discussed above; however, if only the signal band of interest is considered, the number of quantizer harmonics falling in that band can be much smaller (see Fig. 1(d)), and thus so will be the in-band quantization error. Fig. 2 shows an example for a uniform quantizer with 2^n levels, where $n = 12$; as seen, even if the input frequency is 1000 times smaller than the upper band-edge frequency (in which case 1000 harmonics will be present in-band), the total in-band quantization error is significantly smaller than the classical value for sampling plus quantization, assuming no oversampling; this value is indicated in the figure. This advantage is directly due to the fact that, in the absence of sampling, the quantization error is not aliased, and presents a challenge to implement digital signal processors without any sampling. The rest of this paper studies digital signal processors which operate in purely continuous time (CT). A preliminary qualitative description of the main idea has been presented in a brief letter [1] along with experimental results from a rudimentary implementation (a first-order filter with 2-bit coefficients and 4-bit signal quantization). Here we instead present the theoretical justification, and report simulation results from high-order structures with multi-bit signal quantization.

2. PRINCIPLE

We consider as a prototype a classical analog transversal structure [2] consisting of continuous-time delays D and analog multipliers, as shown in Fig. 3. The quantizer at the input will for the moment be ignored. The output of the structure is:

$$y(t) = \sum_{k=0}^{K} a_k w(t - kT) \tag{1}$$

with T being the delay of one delay element. Taking Laplace transforms we obtain:

$$Y(s) = H(e^{sT})W(s) \tag{2}$$

with

$$H(e^{sT}) = \sum_{k=0}^{K} a_k (e^{sT})^{-k} \tag{3}$$

We now assume that $w(t)$ is an adequate representation of the input $x(t)$, quantized to the equivalent of N bits by the quantizer shown, and thus can be represented by:

$$w(t) = \sum_{n=1}^{N} 2^{-n} b_n(t) \tag{4}$$

where $b_n(t)$, $n = 1,...,N$ are binary CT waveforms (henceforth called "bit waveforms"). The representation in (4) is illustrated in Fig. 4. It is emphasized that the bit waveforms, although binary, are functions of continuous time, just as the input signal is. In hardware implementation, such signals can be produced by a continuous-time parallel analog-to-digital converter (ADC) with no clock [3]. No time sampling is involved; the sampling is in the amplitude domain [4-6], since the pre-determined quantization levels w_i and the input waveform determine the transition instants t_i.

From (1) and (4) we obtain:

$$y(t) = \sum_{k=0}^{K} \sum_{n=1}^{N} a_k 2^{-n} b_n(t - kT) \tag{5}$$

which, after interchanging the order of summation, leads to:

$$y(t) = \sum_{n=1}^{N} 2^{-n} \left[\sum_{k=0}^{K} a_k b_n(t - kT) \right] \tag{6}$$

The quantity in brackets represents exactly the same type of processing for b_n, as (1) indicates for w; the coefficients a_k can be implemented digitally (see below). The rest of the expression indicates binary weighting and summation. This can be accomplished by a digital weighted adder using combinational logic. The resulting digital output can be converted to analog form by a digital-to-analog converter (DAC) based on a binary-weighted continuous-time analog adder [3], with no clock.

The operations just discussed can be represented as shown in Fig. 5. From the above derivation it follows that the systems of Figs. 3 and 5 are input-output equivalent. Depending on the times the bit waveforms are changing and the relative times their delayed versions arrive at the adder input, the output can exhibit local non-monotonicity, as shown in Fig. 6 (a very coarse quantization has been used for illustration purposes). For a periodic input, the output quantization error is also periodic, and its spectrum is found only at the same frequencies as those of the input quantization error spectrum. Given that the systems of Figs. 3 and 5 are input-output equivalent as shown above, one may find it easier to deduce some facts about the latter by looking at the former; for example, as follows from Fig. 3, the output quantization error is simply the input quantization error filtered by the same transfer function as the signal itself.

3. DESIGN CONSIDERATIONS

For completeness, we summarize here some hardware design considerations from Ref. 1, and expand on some of them.

The coefficients a_k are implemented by digital words, and are multiplied by single-bit waveforms; thus no multiplications are required, and the bit waveforms $b_n(t - kT)$ can be used to simply gate the coefficient words to the adder. The continuous-time digital delay elements can be implemented in several ways, one of which uses digital inverters in cascade. The delay value for each element can be augmented by extra capacitive loading and by limiting the current driving capability of each inverter, but it must be short enough so that the inverter can completely switch between 0 and 1 within the shortest anticipated interval; from Fig. 4 it is evident that this can be decided from knowledge on the highest rate of change expected at the input. For large T, several inverters have to be placed in cascade, and the value of the total delay fine-tuned by locking it to the period of an external clock through a phase-locked loop. It is stressed that the clock in such a scheme is only used to program the delay value, and in no way does it interfere with the CT operation of the structure.

Depending on the relation between the input frequency and the delay values, the transitions of the various bit waveforms at the input of the adder can differ in time by a very small amount. This places demands on the speed of the adder and DAC, and may limit the proposed technique to low-frequency applications. Limited speed will affect the least significant bit first; for example, the minute up-then-down spike in Fig. 6 may be missed. The result is not serious, as the energy of such spikes is primarily at out-of-band frequencies, and no new frequency components are introduced to the output spectrum. The latter claim can be easily seen in the case of a periodic input: the above spike train will then also be periodic with the period of the input, and its frequency components will be at integer multiples of the input frequency. As the input frequency is raised, the degradation of the quantization error due to such effects is graceful, not only because the in-band energy of such spikes is small, but also because at high input frequencies more and more of the spike harmonics fall out-of-band. Simulations confirm this. Finally, it is stressed that the above errors do not have a lasting effect, since only combinational logic with no memory is used.

Recently proposed non-uniform sampling ADC techniques [5,6] can be employed. In certain of these schemes a clock is used; if the time quantization is sufficiently fine, the resulting pseudo-CT operation can still provide satisfactory results. The structure then becomes basically equivalent to a conventional digital signal processor with a very high degree of oversampling.

4. SIMULATION RESULTS

Various structures have been extensively studied through Matlab/Simulink simulations. A very fine, fixed time step was used, and care was exercised in setting the parameters of Fourier analysis, in order to accurately check the nature of the output spectrum. As an example, we implemented a 28th-order

transversal structure, with unit element delay of $T = 125$ μs and 12-bit input signal quantization. An equiripple passband response was used, combined with a narrow stopband in order to allow most of the frequency components of the input signal quantization error to get through to the output, for illustration purposes. The passband was 0 to 3.3 kHz. The frequency response up to 32 kHz is shown in Fig. 7(a); as seen, it is periodic with period $1/T$ =8 kHz. This is to be expected, since (3) is identical to the z-transform transfer function of a corresponding discrete-time filter, with z replaced by e^{sT}. The output spectrum for a sinusoidal input of 1 kHz is shown in Fig. 7(b). As expected from the above discussion, the quantization error components are found only at multiples of the input frequency (in fact, only odd harmonics are found, due to the symmetry of the quantizer characteristic around the origin). This causes the total in-band quantization signal to be only -120 dB (referred to the input rms value) with the 12 bit quantization used, consistent with Fig. 2. This error increases to -106 dB when the input signal frequency is decreased to 100 Hz. When the input is changed to 5 kHz, the output spectrum becomes as shown in Fig. 7(c). A classical discrete-time filter with the same frequency response (based on 8 kHz sampling) would have produced an alias component at 3 kHz; however, in the case of the CT version it is seen that no such aliasing is produced; indeed, as expected from the theory presented above, neither signal aliasing nor quantization error aliasing are observed, and in fact there is no in-band quantization error in this case.

5. CONCLUSIONS

Analysis and simulations, presented here, and supported with experimental evidence presented in Ref. 1, suggest that continuous-time digital signal processing is possible, and that it presents several advantages in comparison to the classical, discrete-time case: (a) No signal aliasing; (b) No quantization error aliasing; this avoids sub-harmonic components, and reduces the in-band quantization error power. Despite the continuous-time operation, the technique is digital, with all signals inside the processor being binary-valued, and thus it shares with discrete-time signal processing the advantage of noise immunity in hardware implementations. The technique shares with the discrete-time case the property that the frequency response is periodic. The approach places demands on the speed of the adder and DAC used, which may limit the frequency capability of the technique and, in any case, represents a hardware design challenge. The extent to which this challenge can be met can only be determined via a full-blown hardware implementation.

6. REFERENCES

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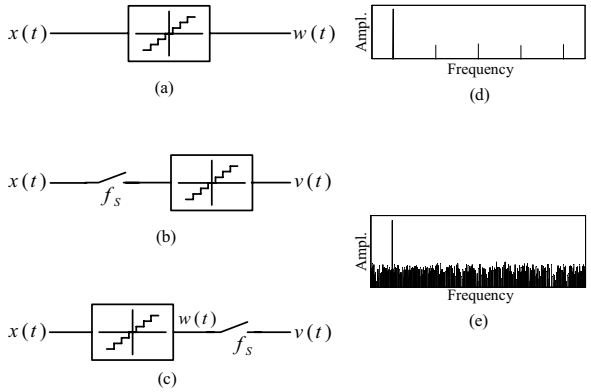

Fig. 1 (a) Quantizer, (b) Sampler and quantizer, (c) System in principle equivalent to (b); (d) Output spectrum for (a); (e) Output spectrum for (b) and (c).

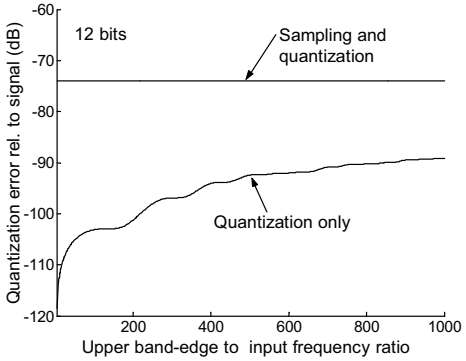

Fig. 2 Quantization (12 bit) error power relative to signal power for a sinusoidal input, as a function of the ratio of upper band-edge frequency to input frequency. No oversampling is assumed in the case of sampling and quantization.

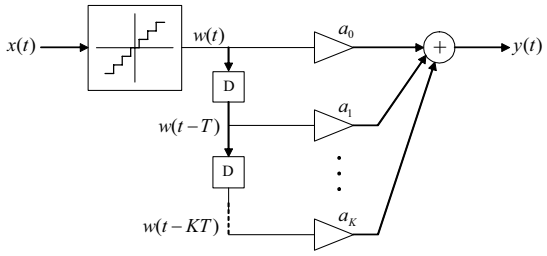

Fig. 3 Analog transversal structure based on continuous-time delay elements, preceded by a quantizer.

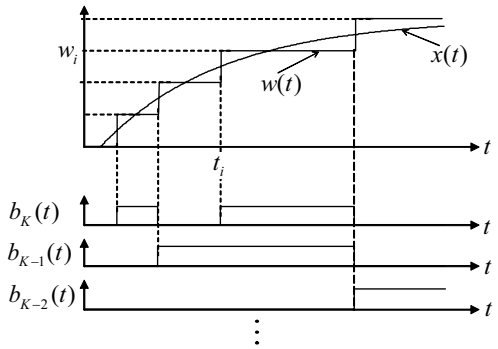

Fig. 4 A CT (continuous-time) signal $x(t)$, its uniformly quantized version $w(t)$, and the CT digital representation of $w(t)$ in terms of CT bit waveforms.

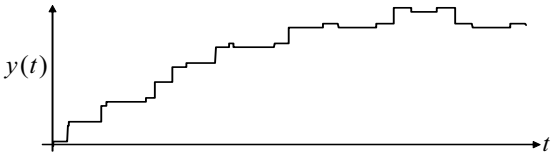

Fig. 6 Typical output waveform for the systems in Figs. 3 and 5; a very coarse quantization is used for illustration purposes.

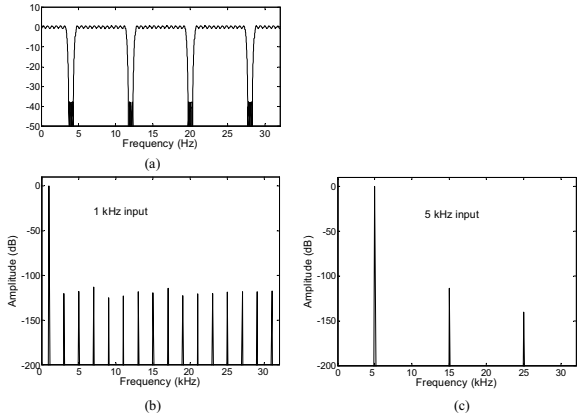

Fig. 7 Simulation results for a 28-tap low-pass transversal structure using 125 μs delay elements with 12-bit input quantization, with a 3.3 kHz passband. (a) Frequency response, (b) Output with 1 kHz input, (c) Output with 5 kHz input.

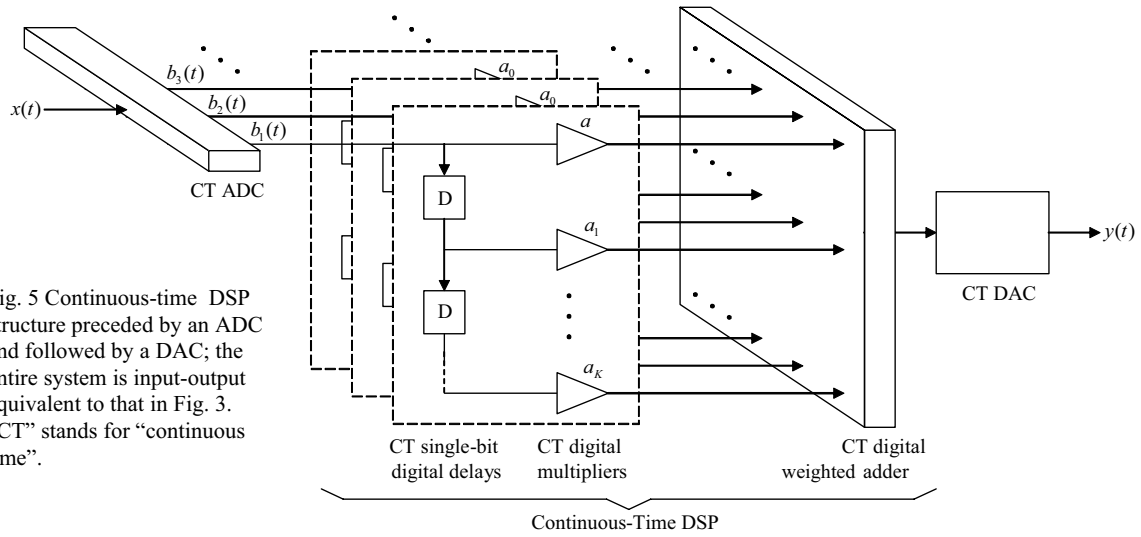

Fig. 5 Continuous-time DSP structure preceded by an ADC and followed by a DAC; the entire system is input-output equivalent to that in Fig. 3. "CT" stands for "continuous time".