A HIGH-PERFORMANCE MULTI-PURPOSE DSP ARCHITECTURE FOR SIGNAL PROCESSING RESEARCH

Scott A. Morrison, Jeremy S. Parks, Karl S. Gugel

Applied Digital Design Laboratory (www.add.ece.ufl.edu)
The University of Florida, Gainesville, Florida, 32611, USA
Email: scott.morrison@ieee.org, jeremyp@ufl.edu, gugel@ecel.ufl.edu

ABSTRACT

This paper presents a powerful and flexible Digital Signal Processing (DSP) architecture based on the Texas Instruments TMS320VC33 DSP and high speed PCI bus. The DSP board provides a convenient, flexible means to test signal processing algorithms in real-time hardware. Algorithms implemented for several research projects include Normalized Least Mean Square (NLMS) Adaptive Filter, Recurrent Neural Network (RNN), Viterbi Decoding, and Adaptive Beamforming. The low-cost, re-configurable system is presently being used in various research projects such as multiple channel sampling and filtering MEMS-based Acoustic Arrays, Wireless LAN hardware implementation, and neural net classification of primate EEG waveforms. The paper provides a detailed description of the DSP board, the theory behind its selection of components, and how it is being used in the earlier mentioned research projects.

1. INTRODUCTION

Research into cutting-edge DSP solutions for real-world problems has led to new mathematical models and their applications. Until recently, this research has primarily been conducted using simulation tools such as Matlab without the researcher applying the new methods in DSP hardware. The reason for this is simple—the prohibitive cost of custom DSP hardware to fit a particular project.

Increasingly, university research-sponsors are requiring hardware implementation of the final DSP algorithms. Therefore, researchers seek to bridge the gap between software simulations and hardware implementations. Rapid-prototype environments are used in academia and industry for this purpose [1]. These prototype environments usually consist of software simulators, system-design tools, code composers and assembly tools, and a general-purpose Printed Circuit Board (PCB) containing some combination of DSPs, FPGAs, and other interface hardware [2].

Commercially available Rapid-Prototype Boards that work for a particular research project may not be flexible enough to meet the needs of other research projects with different hardware requirements. To avoid buying different DSP hardware boards to suit each project, a single, multi-purpose DSP architecture is desired. Using a common hardware platform also facilitates the sharing of resources among projects. This flattens the learning curve for researchers starting new projects.

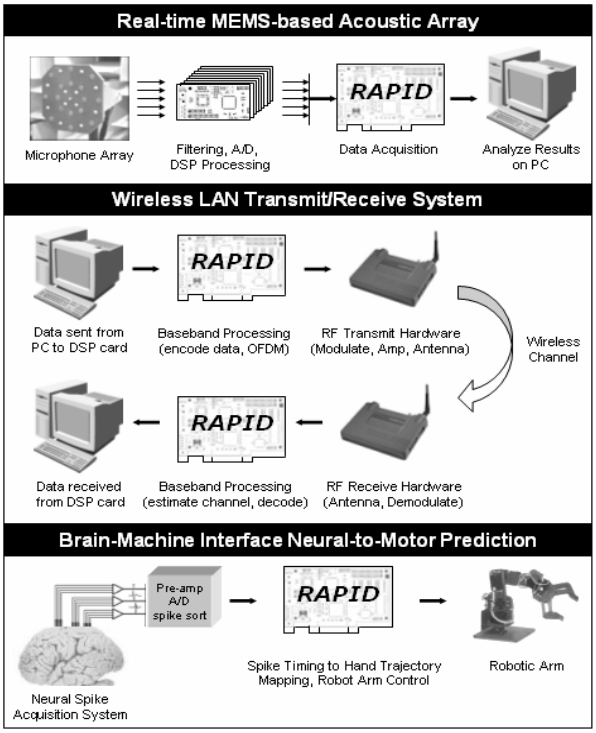

Figure 1. System implementations using the RAPID Board.

At The University of Florida (UF), the solution to this problem was to develop a DSP platform for signal processing research having a flexible architecture at a low-cost, which encourages its widespread use on multiple projects.

In this paper, we present a multi-purpose DSP board known as the **R**eal-time **A**rchitecture for **P**rototyping and **I**mplementation of **D**igital Signal Processing (RAPID). Hardware and software for this DSP environment will be discussed, as well as the application of the RAPID Board to three different research projects—MEMS-based Acoustic Arrays, Wireless LANs, and a Brain-Machine Interface (See Figure 1).

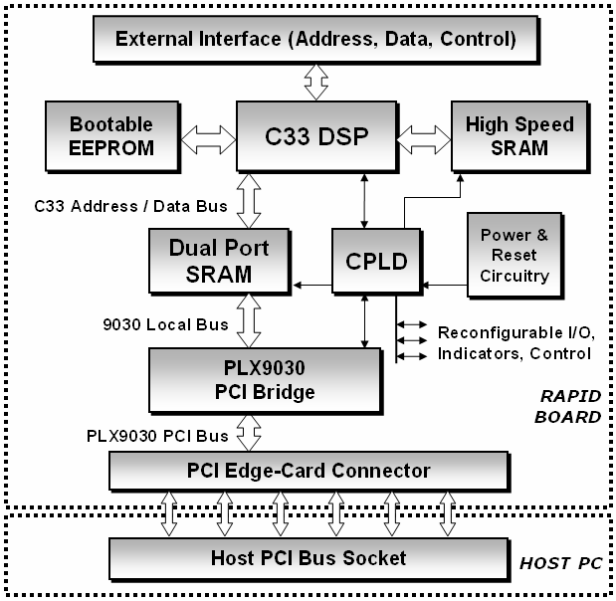

Figure 2. RAPID Board Architecture.

2. RAPID BOARD HARDWARE

For the RAPID Board to fit a number of research projects, the following list of general requirements was used to guide hardware development:

- Fast, general-purpose digital signal processor.
- Ample high-speed SRAM for program and data storage.
- Dual mode operation: PC-mode for fast data transfer and program monitoring, or Standalone-mode for field operation and system integration.
- Reconfigurable control and flexible peripheral interfaces.

The following sections describe the chosen hardware for the RAPID Board based upon the criteria above (See Figure 2).

2.1. TMS320VC33 DSP

In order to support high-speed DSP applications as well as preserve flexibility throughout the various research projects, the selection of the DSP chip was based upon the following criteria:

- Fast 32-bit floating-point processing
- Full-featured instruction set
- Multiple timers and interrupts, DMA
- Large internal SRAM
- Low-power and low-cost

The Texas Instruments TMS320VC33 DSP was found to meet all the above criteria [3]. The 75MHz floating-point processor performs 75 MIPS and 150 MFLOPS, operating at 3.3V with power consumption less than 200mW. In addition to the 136KB of internal SRAM, this processor offers hardware loop control, DMA, and four hardware interrupts. Besides the $15 low-cost, another advantage for choosing this DSP was the plentiful online support tools and libraries provided by Texas Instruments [4].

2.2. PCI Interface and Dual-Port SRAM

Some research projects require fast data transfer to and from a PC. The PC-DSP connection allows a convenient interface to the board during testing, though it is not necessarily required in the final product. The PCI Bus was chosen to interface the RAPID Board because of its high-speed 32-bit transfer and DMA capabilities, and the PLX9030 PCI SMARTarget I/O Accelerator was chosen to provide this interface. Data exchange between the PLX9030 and the C33 DSP is performed through 4K by 32 bits of high-speed Dual Port SRAM (DPRAM).

2.3. SRAM and Expansion

In addition to the generous DSP internal SRAM, some DSP solutions require large additional amounts of memory for data storage and computations. A survey of candidate projects indicated that as much as 2-4MB of additional memory might be needed. Consequently, fast 15ns SRAM produced by Cypress Semiconductor (Part Number CY7C1049B-15VC) was selected to yield a total of 512k by 32bits, or 4MB, of external memory.

The DSP data bus and address bus were made available on header pins for connection to additional hardware such as FPGAs, as may be required for various architectures. Bus control signals were also included on this header to help the user interface easily to the DSP. In addition to this general-purpose data interface, the C33 serial port was made available to a DB15 connector. This serial port could interface peripherals such as ADCs and DACs, as well as another C33 DSP should a multiprocessor system be required.

2.4. Control

Control signals from the major components of the RAPID Board—namely the DSP, SRAM, DPRAM, PCI Bridge, and External Interface—were logically glued together with an Altera CPLD (Part Number EPM3032A). With a maximum 4.5ns pin-to-pin logic delay, this reprogrammable control solution allows users to customize the DSP memory map and peripheral connections. Reprogramming is done through the CPLD JTAG port using Altera's HDL Design Software.

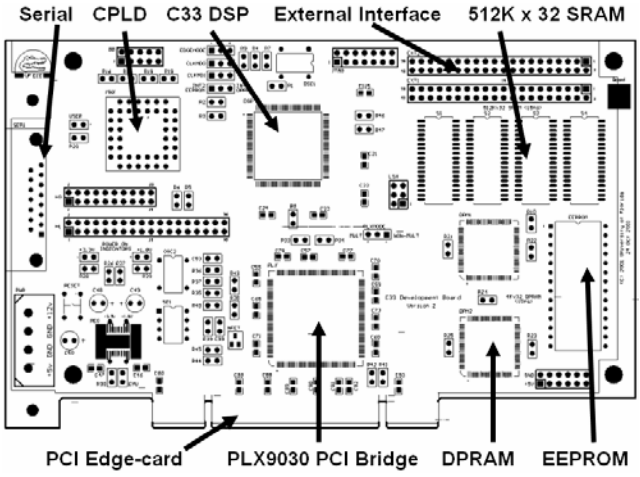

Figure 3. PCB Layout of RAPID Board

3. SOFTWARE TOOLS

In PC-mode, the RAPID Board is interfaced through a Windows C-based console program using function calls to the PLX9030 API. The console program provides a user interface that controls the PLX registers and settings, access to the DSP's memory and functions, as well as various test routines. Its functionality includes:

- Read / Write PLX PCI Configuration Registers
- Reset the DSP Board
- Read/Write DSP Memory and store contents to file in Hex, Integer, or Float format
- Download programs and operating system to DSP
- Execute programs in DSP memory

To support PC-mode development, the DSP runs an Operating System (OS) written in Texas Instruments C3x Assembly Language [5]. The DSP OS communicates with the PC Console Program via the DPRAM. The DSP OS can load and execute program code in internal memory or the external SRAM, as well as allow the user to read and write to DSP registers and memory.

The DSP OS, as provided from the PC Console Program, is booted from the DPRAM in PC-mode. This allows the user to change the operating system without burning expensive EPROMs. For applications where the board will be used without a PC, the DSP is booted in Standalone-mode from the EPROM. The user may select between PC-mode and Standalone-mode via a jumper on the board.

4. MATLAB DEVELOPMENT LINK

Matlab or similar programs are often used to develop software models and simulations of a system before implementation in hardware. These tools may also be used to validate the prototype DSP architecture. Using the same input data, results from computer simulations can be compared with results of the DSP system. To aid this process, a Matlab interface was developed that is capable of accessing the RAPID Board via Matlab function calls. The Matlab/RAPID Board link allows Matlab scripts to initialize the board, read memory, and download and execute programs. This allows seamless data flow between Matlab and the board, which bridges the gap between simulation and implementation.

A real-time Spectrum Analyzer research tool was created using the Matlab/RAPID Board link. The analog signal source was sampled through an ADC connected to the RAPID Board external interface. Matlab reads the sampled data through the RAPID Board link, then displays the frequency spectrum of the signal in real-time (See Figure 4). This tool was used to develop the MEMS-based Acoustic Array project discussed in section 5.1.

5. REAL-TIME SYSTEM IMPLEMENTATIONS

The flexibility and functionality of the RAPID Board has allowed for its use in many signal processing research projects at UF. This is highlighted in the diversity of the first three research projects to use the RAPID Board, as described in the following sections.

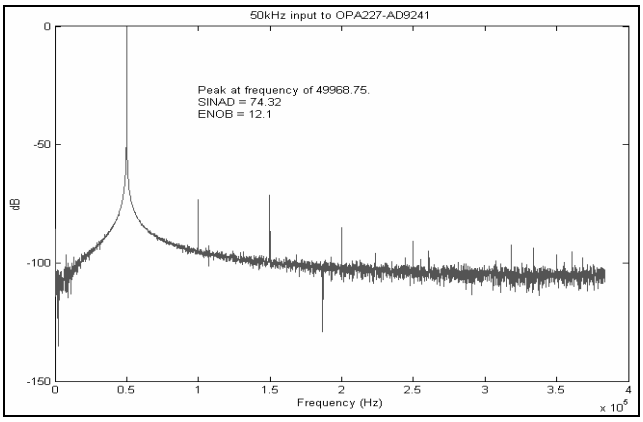

Figure 4. Real-time Spectrum Analyzer using the Matlab link.

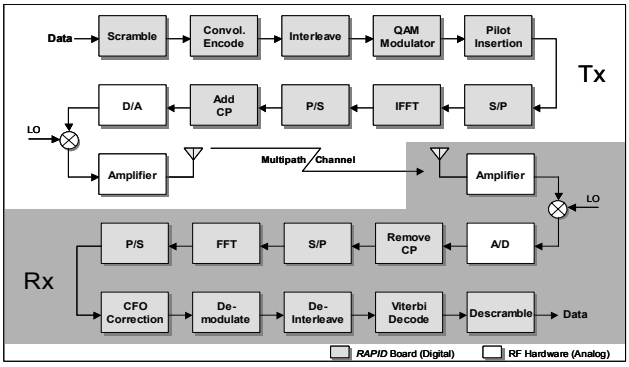

Figure 5. WLAN Transmit/Receive System

5.1. MEMS-based Acoustic Array

The MEMS-based Acoustic Array project is a real-time signal processing system designed to sample and process data from a 16-channel acoustic array used in wind tunnels. Real-time beamforming algorithms will be applied to the data, thereby producing an acoustic energy "map" that will assist in locating sources of noise in airframes [6]. The RAPID Board will be used to develop and test beamforming and FFT code for the eventual 24-DSP hardware system (See Figure 1). Further processing will be performed by an additional RAPID Board interfacing the PC. The system provides a useful tool for engineers attempting to reduce noise pollution caused by airplanes.

5.2. Wireless LAN

Wireless LAN (WLAN) products continue to gain popularity as new standards push data rates. Although IEEE 802.11b is the predominant standard in the United States—delivering data rates up to 11 Mbps—products using the IEEE 802.11a standard promise data rates approaching 54Mbps [7]. The 802.11a standard specifies the use of Orthogonal Frequency Division Multiplexing, which splits the data into multiple orthogonal subcarriers in the 5 GHz frequency band.

The goal of the WLAN project is to produce a complete transmit/receive wireless LAN system that employs the 802.11a standard. Two RAPID Boards will be used in this project to perform baseband processing on both the transmit and receive sides (See Figure 1). Baseband processing refers to the

preparation of the data before and after the RF transmission to protect against errors that are incurred by the wireless channel. This includes encoding and decoding the data, modulation, channel estimation, etc., as shown in Figure 5. Several of these components have been designed using the RAPID Board, including the Viterbi decoding block. The results showed that the RAPID Board performed the Viterbi decoding calculations on 100 octets of data in 50µs, as compared to 6.19s on a 500MHz PC. This is a speedup of 124x.

In collaboration with UF, the Wireless Antenna and Microwave Lab at the University of South Florida will manage the RF portion of the project. The complete system will be used for further testing and algorithm development, such as the effects of additional antennas or different modulation techniques on the overall system.

5.3. Brain-Machine Interface

At Duke University (Dr. Miguel A.L. Nicolelis, *et al*.), ensembles of cortical neurons were observed with a large array of microelectrodes implanted in the pre-motor and motor regions of a primate brain [8]. Spike detection and sorting algorithms process the microelectrode outputs to determine firings of single neurons (See Figure 1). While the firing information was collected, a sensor recorded the 3D hand-position of the primate performing various tasks. Researchers at UF have identified linear and non-linear mapping algorithms to predict hand movement from the spike data [9].

The RAPID Board has been used to implement the neural-to-motor mapping algorithms—specifically, the Normalized Least Mean Square (NLMS) Adaptive Filter and the Recurrent Neural Network (RNN). With neuron firings collected into 100ms time bins, the RAPID Board running at 75MHz processes a 104-input 10-tap FIR trained with NLMS in precisely 220.0µs. Using the same data, the feed-forward RNN takes 35.1µs (See Figure 6).

These DSP implementations provide 3D hand trajectory prediction in real-time. The evolution of this project will see the same RAPID Board in standalone mode connected to a robot arm to mimic the real-time movements of the primate. The flexible CPLD control and data interface will permit easy connection to the robot arm as well as a sensory-feedback system in the future.

6. CONCLUSION

A high-performance DSP architecture was presented that provides a low-cost solution to an assortment of signal processing applications. The fast PCI bus interface, large external SRAM, and customizable peripheral interfacing allow the RAPID Board to fit the needs of varied project requirements. This was demonstrated through its successful implementation in multiple channel sampling and filtering MEMS-based Acoustic Arrays, Wireless LAN hardware implementation, and neural net classification of primate EEG waveforms.

Using a single DSP architecture across various projects allows the sharing of code and resources, which shortens the development time for future researchers. In the future, an FPGA daughtercard will be connected to the RAPID Board for greater system flexibility of DSP implementations.

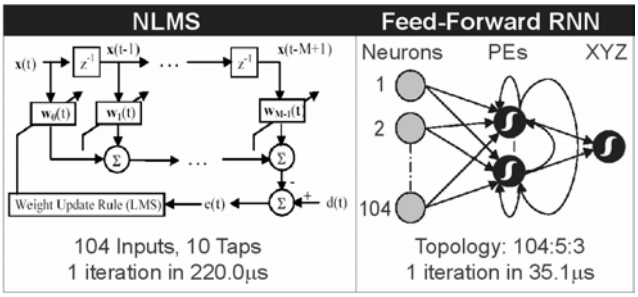

Figure 6. Brain-Machine Interface Signal Processing Results

ACKNOWLEDGEMENTS

The authors would like to acknowledge Joel Fuster, UF Research Assistant, for his work with the Matlab/RAPID Board link. The RAPID Board development was supported in part by grants from the National Science Foundation (#0097636 and #0097114) and the Defense Advanced Research Projects Agency (N-66001-02-C-8022).

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