AN ASYNCHRONOUS SAMPLE-RATE CONVERTER FROM CD TO DAT

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ABSTRACT

When the input and the output clocks are asynchronous, the nearest interpolated value can be used to approximate the desired output sample. The design for an asynchronous sample rate conversion (ASRC) from 44.1kHz compact disk to 48kHz digital audio tape is presented. Using wave digital filter and a fractional delay filter, the ASRC is implemented in all-digital form. To this end, this paper proposes a novel IIR fractional delay filter. Compared with other methods, the proposed method requires less hardware complexity and obtains signal-quality compatible with digital audio.

1. INTRODUCTION

There is a need for simple digital interfacing between different digital audio equipments. Compact disc (CD) and digital audio tape (DAT) formats are now widely accepted as very reliable and high quality means of reproducing music. Because it is very difficult to obtain good performance in converting of these formats, several methods have been proposed to address this issue.

The simplest method is to convert the input samples into analog and resample the analog signal to the desired sampling rate using the DAC and ADC. However, this introduces the harmonics and noise distortion, and decreases the overall performance of the system. A multirate technique (*M:N*) is the most popular method of sample rate conversion. However, in the application of CD and DAT, it is not applicable. The fixed ratio *M/N* is 160/147. Thus the sampling rate of the input signal is interpolated by a factor of 160, and decimated by a factor of 147. This approach requires more computation and more hardware. Using the sinc function, this method generates a fractionally sampled signal for the sampling rate conversion [1]. However, this method needs a very big look-up table to store the 80×63 coefficients.

We can efficiently design this rate converter if we use a fractional delay (FD) filter to reduce the number of the filter coefficients. The Farrow structure is one of the most widely known FIR-based FD filter [2][3]. However, in the application from CD to DAT, we can achieve a good performance when we use a third order FIR fractional delay filter with 192-taps [4].

In this paper, a new IIR fractional delay filter structure is proposed to reduce the number of required coefficients. To obtain sufficient accuracy, we use a third order IIR fractional delay filter. Using this IIR fractional delay filter, an efficient algorithm of ASRC is proposed.

In Section 2, the new IIR fractional delay filter is proposed. In Section 3, the implementation of ASRC from CD to DAT is given using IIR FD filter. Simulation results are presented in Section 4. Finally, conclusions are drawn in Section 5.

2. IIR FACTIONAL DELAY FILTER

The general transfer function of an allpass filter can be expressed as

$$H(z) = \frac{B(z)}{A(z)} = \frac{z^{-N} A(z^{-1})}{A(z)}, \qquad (1)$$

where $A(z) = \sum_{n=0}^{N} a_n z^{-n}$ and $a_0 = 1$.

In order to control the delay of an allpass filter with a single delay parameter d, each filter coefficient a_n can be approximated using L-th order polynomial as

$$a_n = \sum_{l=0}^{L} e_{ln} d^l, \qquad n = 0,1,...,N. \qquad (2)$$

The coefficients e_{ln} for each coefficient a_n can be determined by Thiran formulas [5][6] as

$$\begin{aligned} a_k &= (-1)^k \binom{N}{k} \prod_{n=0}^{N} \frac{d+n}{d+k+n}, \\ &= (-1)^k \binom{N}{k} \prod_{n=0}^{k-1} \frac{d+n}{d+N+n+1}, \end{aligned} \qquad (3)$$

where $\binom{N}{k} = \frac{N!}{k!(N-k)!}$.

The coefficient a_k is expressed as a rational polynomial of the fractional delay d. Since it is difficult to implement the division including a time-varying factor, we need to transform the coefficients to a polynomial form.

The modified coefficient $\hat{a}_k$ is obtained by multiplying a common factor to each coefficient a_k as

$$\begin{aligned}\hat{a}_k &= (-1)^k \binom{N}{k} \frac{\prod_{n=0}^{k-1}(d+n)}{\prod_{n=1}^{k}(d+N+n)} \prod_{n=1}^{N}(d+N+n), \\ &= (-1)^k \binom{N}{k} \prod_{n=0}^{k-1}(d+n) \prod_{n=k+1\le N}^{N}(d+N+n), \\ &\cong \sum_{l=1}^{N} \hat{e}_{lk} d^l, \qquad \text{for } k = 1,2,\cdots,N,\end{aligned} \tag{4}$$

where $a_0 = 1$.

The canceling division $g(d)$ can be approximated by a polynomial in fractional delay d:

$$g(d) = \frac{1}{\prod_{n=1}^{N}(d+N+n)} \cong \sum_{i=0}^{I} g_i d^i \,. \tag{5}$$

The coefficient g_i is approximated by the truncated Maclaurin series or Talyor series expansion as

$$g(d) \cong \frac{N!}{(2N)!} \prod_{n=1}^{N} \left[1 + \sum_{k=1}^{I} (-1)^k \left(\frac{d}{N+n} \right)^k \right], \tag{6}$$

where I is the order of the approximating polynomial.

However, the difference between the values of $\hat{a}_k$ and the values of $g(d)$ is about 10^2 times in second order case and about 10^4 times in third order case. Thus large word-lengths are needed for VLSI implementation of the filter structure. To solve these problems, a modified allpass filter structure is proposed.

The transfer function of an allpass filter can be expressed as

$$H(z) = \frac{g(d)[\hat{a}_N + \cdots + \hat{a}_1 z^{-(N-1)}] + z^{-N}}{1 + g(d)[\hat{a}_1 z^{-1} + \cdots + \hat{a}_N z^{-N}]}. \tag{7}$$

Each coefficient a_k of the IIR filter is

$$\begin{aligned}a_k &= g(d) \cdot \hat{a}_k, \\ &= \left[\sum_{i=0}^{I} g_i d^i \right] \cdot \left[\sum_{l=1}^{N} \hat{e}_{lk} d^l \right].\end{aligned} \tag{8}$$

It can be noticed that d^l is close to zero when l is large since the range of the delay parameter d is from -0.5 to 0.5. Thus a_k can be approximated as

$$\begin{aligned}a_k &= g(d) \cdot \hat{a}_k, \\ &\cong \sum_{m=1}^{M} \left[\sum_{l=1}^{m} g_{m-l} \hat{e}_{lk} \right] d^m,\end{aligned} \tag{9}$$

where $a_0 = 1$.

Using the coefficient approximation of (9), $A(z)$ can be expressed as

$$\begin{aligned}A(z) &= 1 + \sum_{n=1}^{N} a_n z^{-n}, \\ &= 1 + \sum_{n=1}^{N} \left[\sum_{m=1}^{M} \left(\sum_{l=1}^{m} g_{m-l} \hat{e}_{\ln} \right) d^m \right] z^{-n}, \\ &= 1 + \sum_{m=1}^{M} \left[\sum_{n=1}^{N} \left(\sum_{l=1}^{m} g_{m-l} \hat{e}_{\ln} \right) z^{-n} \right] d^m, \\ &= 1 + \sum_{m=1}^{M} \left[\sum_{n=1}^{N} c_{mn} z^{-n} \right] d^m.\end{aligned} \tag{10}$$

In (10), $c_{mn} = \sum_{l=1}^{m} g_{m-l} \hat{e}_{ln}$ is a constant value.

We can get the corresponding difference equation in the time domain directly as

$$y(k) = x(k-N) + \sum_{m=1}^{M} \left\{ \sum_{n=1}^{N} \left[x(n+k-N) - y(k-n) \right] c_{mn} \right\} d^m. \tag{11}$$

The third order structure obtained by the proposed method is shown in Fig. 1.

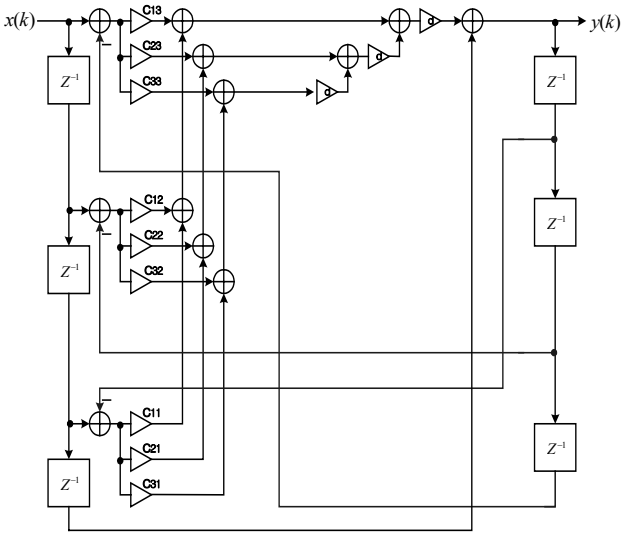

Fig. 1. Proposed structure of third order IIR FD filter.

3. IMPLEMENTATION

Using the third order IIR fractional delay filter shown in Fig. 1, we can get the implementation of asynchronous sample rate converter from CD to DAT as shown in Fig. 2.

In the application of ASRC from CD to DAT, each input sample is interpolated by a factor of two to maintain some requisite fidelity. For the digital implementation of the whole system, we can use the wave digital filter shown in Fig. 3 instead of interpolator and LPF.

Fig. 4 shows an example of the input and output timing relationship when the output sampling rate is greater than the input sampling rate. When $y(0)$ is ready to output, $x(0)$ can be shifted to buffer because the timing difference between input sample and output sample is zero in Fig. 4 (a) and (b). However, if we interpolate the input sample, when $y(1)$ is ready to output, the fractional delay d_1 of Fig. 4 (b) is smaller than of (a). So we can obtain the signal quality compatible with digital audio using a structure of third order IIR fractional delay filter.

Also in the process of storing the data in the buffer and shifting it, we can choose the interpolated sample, which is the nearest position with the output sample instead of the last sample in Fig. 4 (c). Then we can reduce the range of the estimation error of the fractional delay once again.

The fractional delay d doesn't need to be computed every time, as a new sample gets into the delay line of the fractional delay filter. In the application from CD to DAT, we need to do a onetime computation of the delay parameter d and the shift parameter s, which match the output sample rate 48kHz and the input sample rate 44.1kHz. This computation is based on the fact that the filter generates 80 output samples per every 147 input samples:

for $n = 0:79$

$$s_n = \left\lfloor (n-3)\frac{147}{80} \right\rfloor - \left\lfloor (n-4)\frac{147}{80} \right\rfloor$$

$$d_n = n\frac{147}{80} - \left\lfloor n\frac{147}{80} \right\rfloor$$

if $(d_n >= 0.5)$ then

$$d_n = d_n - 1$$

end

end

where $\lfloor x \rfloor$ stands for the integer part of x.

In order to reduce the processing of d and s, they can be replaced with look-up tables which have 80 values.

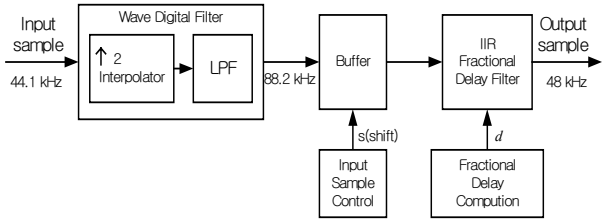

Fig. 2. Proposed structure for ASRC from CD to DAT.

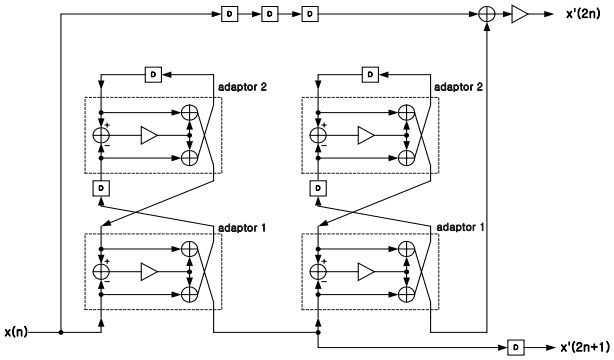

Fig. 3. Wave digital filter.

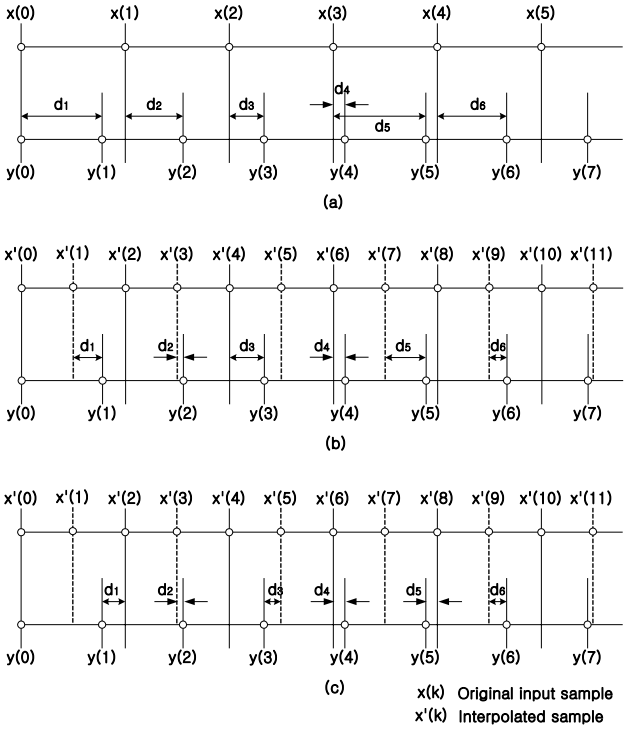

Fig. 4. Input and output timing relationship.

4. SIMULATION RESULTS

In this paper, a novel structure of IIR fractional delay filter has been presented. Using this structure, we can get an asynchronous sample rate converter from CD to DAT.

In the application for CD and DAT, the delay parameter value of Fig. 5 is used for obtaining the output of the ASRC. We compare the conventional structure of third order FIR filter with 8-taps and the proposed structure of third order IIR filter with 3-taps.

Fig. 6 shows the absolute error for each sample. Fig. 6 (a) shows the output error of third order IIR filter and, Fig. 6 (b) shows the output error of third order FIR filter.

In proposed structure of ASRC, MSE equals 4.05×10^{-8}. And in conventional structure of ASRC, MSE equals 1.05×10^{-7}. We can see than error is reduced by 2 times.

Table 1 compares hardware for third order conventional FIR filter and proposed IIR filter in the same condition. While maintaining low error, the required hardware is reduced by 70%.

5. CONCLUSIONS

In this paper, the digital ASRC technique has been presented by using the wave digital filter and fractional delay filter. We have also proposed a new design method for IIR fractional delay filter. By simulations, it was shown that the proposed ASRC of IIR fractional delay filter requires much less hardware complexity and has better performance.

6. REFERENCES

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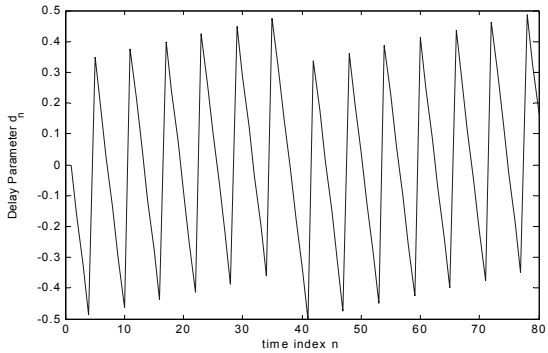
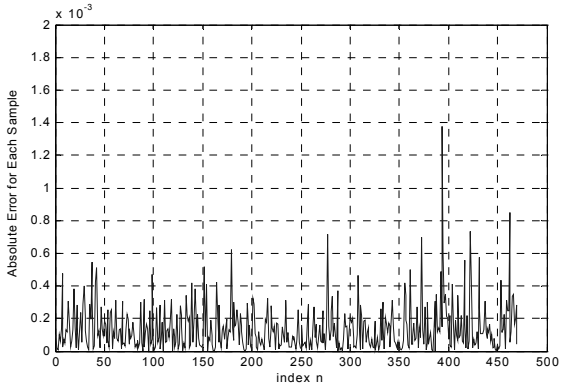
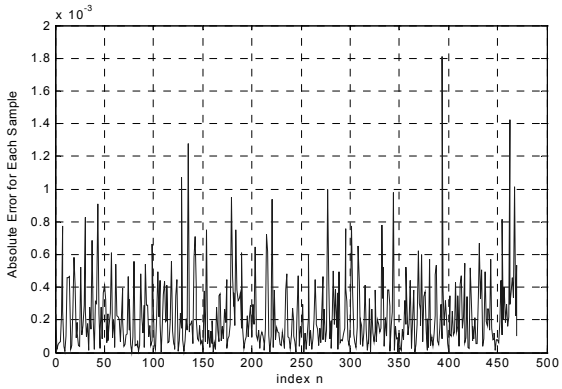


Fig. 5. Delay parameter *d* vs time.



(a)



(b)

Fig. 6. Absolute error for each sample (a) ASRC with a 3×3 tap IIR filter (b) ASRC with a 4×8 tap FIR filter.

Table 1. H/W comparison of conventional FIR filter and proposed IIR filter.

	Delay Element	Multiplier	Adder
IIR filter with 3×3 taps	6	12	12
FIR filter with 4×8 taps	28	35	31