TEMPOREL AND SPECTRAL ANALYSIS OF TIME INTERLEAVED HIGH PASS SIGMA DELTA CONVERTER

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ABSTRACT

Delta sigma modulators are widely used for low to moderate rate analog-to-digital conversion. But they are not adapted to high rate conversion because of time over-sampling requirement. Parallel architecture is a potential solution to increase the frequency range of ΔΣ ADC, especially the time-interleaved high-pass ΔΣ converter. In this paper, we analyze the immunity from low-frequency offered by the high-pass ΔΣ modulators in time-interleaved ΔΣ ADC. The high-pass ΔΣ modulators not only retains the performance of the converter and eliminates low frequency noise, but also allows simple adaptive channel gain equalization scheme to minimize channel gain mismatch effects by using LMS algorithm.

1. INTRODUCTION

ΔΣ A/D conversion techniques have become popular for applications requiring high resolution ADCs. Efforts to extend the frequency range of ΔΣ ADCs have involved the development of high order modulators or the use of multi-bit internal quantizers. However the first ones are more difficult to design because of instability problem and later ones introduce non-linearity in the feedback path that limits the overall resolution. Recently, several approaches using parallelism have been presented to increase the bandwidth of ΔΣ ADCs, in particular the time-interleaved (TI) high-pass ΔΣ architecture [1,2]. This paper analyzes this kind of architecture. The use of high-pass modulators instead of low-pass modulators in such an architecture eliminates the characteristic problem of parallel architecture which is channel mismatch. High-pass modulators remove the effect of low frequency noise, so channel offset in every channels, then in absence of offset effects, a simple but efficient gain equalization technique is used to minimize the effects of channel gain mismatch.

2. ARCHITECTURE

A simple structure of the TI high-pass ΔΣ ADC architecture is shown in Figure. 1. It consists of *M* parallel channels of high-pass ΔΣ modulators and high-pass channel filters that all operate on the input signal, $x[n]$.

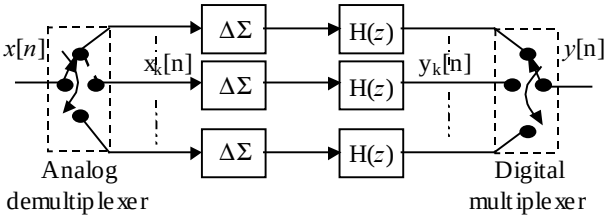

Figure 1. Interleaved ΔΣ ADC architecture

Although the input to each modulator is sampled at $1/M$ the clock rate, each modulator still operates at the full rate. The modulator input is indeed grounded during (M-1) clock cycles and the signal applied during one cycle over M. Otherwise the input to the k-th modulator can be written as

$$x_k[n] = \begin{cases} x[n] & \text{if } n-k \text{ is a multiple of M} \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

If we assume that

$$u_k[n] = \begin{cases} 1 & \text{if } n-k \text{ is a multiple of M} \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

then we have

$$x_k[n] = x[n]u_k[n] \quad (3)$$

The overall output y[n] can be written as

$$y[n] = y_k[n]u_k[n-k_0] \quad (4)$$

where k_0 is a parameter of the architecture. This operation is nothing else that an down-sampling and an interpolation.

In general, the output of the ΔΣ modulator is a quantized sequence that is considered as the sum of a signal component, a quantization error component and a non-ideal error component. Therefore, as depicted in Figure 2, a ΔΣ modulator is equivalent to a linear-time-invariant (LTI) filter, shown as S(z), plus an additive quantization error shown as $e_k[n]$ filtered by N(z) and plus a non-ideal error component shown as $e_{ni}[n]$. S(z) and N(z) are signal transfer function and quantization noise transfer function of the ΔΣ modulator respectively. The high-pass ΣΔ modulator is based on the exact same principle as the low-pass ΣΔ modulator i.e. the quantization noise is shaped away from the signal band by the loop filter [3,4].

The only difference being the position of the signal band, which is now located as $f_S/2$ where f_S is the sampling frequency, compared with a pass-band at dc for the low-pass ΣΔ modulator. Ideally for a L^{th} order high-pass ΔΣ modulator, we have [3,4]

$$S(z)=(-z)^{-L} \quad \text{and} \quad N(z)=\left(1+z^{-1}\right)^{L} \tag{5}$$

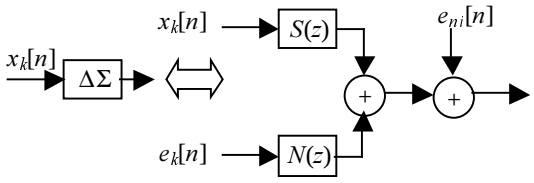

Figure 2. ΔΣ modulator error model

Therefore the overall output is the sum of overall signal component, the overall quantization error component and the overall non-ideal error component. That is

$$y[n]=w[n]+e_q[n]+e_{ni}[n] \tag{6}$$

where $w[n], e_q[n], e_{ni}[n]$ denote the overall signal component, the overall quantization error component and the overall non-ideal error component respectively. The overall non-ideal error component is due mainly to channel mismatch, such as channel gain mismatch and offset mismatch. In absence of the non-ideal error, by the superposition, the overall signal component can be calculated be considering the quantization errors from the ΔΣ modulators to be zero and vice versa.

3. THEORETICAL PERFORMANCE

3.1. Overall signal component

Consider the i-th channel of the architecture with the quantization error source set to zero. Let q[n] = s[n]*h[n] where h[n] is the impulse response of H(z). The output of this channel can be written as

$$t_i[n]=\sum_{k=0}^{\infty} q[n]x[n-k]u_i[n-k]u_i[n-k_0] \tag{7}$$

where $u_i[n]$ is defined by (2). The overall signal component is just the sum of the M $t_i[n]$ sequences :

$$w[n]=\sum_{i=0}^{M-1} t_i[n]=\sum_{k=0}^{\infty} q[n]x[n-k]\sum_{i=0}^{M-1} u_i[n-k]u_i[n-k_0] \tag{8}$$

It follows that

$$\sum_{i=0}^{M-1} u_i[n-k]u_i[n-k_0]=C_M[k-k_0] \tag{9}$$

where

$$C_M[n]=\begin{cases}1 & \text{if } n \text{ is a multiple of M}\\ 0 & \text{otherwise}\end{cases} \tag{10}$$

So (8) becomes

$$w[n]=\sum_{k=0}^{\infty} q[k]x[n-k]C_M[k-k_0] \tag{11}$$

Hence,

$$w[n] = x[n] * h'[n], \tag{12}$$

where

$$h'[n] = C_M[n-k_0]\{s[n] * h[n]\} \tag{13}$$

Assume that $S(z)$ is a L-th order high-pass ΔΣ modulator, and $H(z)$ is a FIR filter. Specially $s[n] = (-1)^L\delta[n-L]$ and $h[n] = 0$ when $n < 0$ or $n \geq N$. So , (13) becomes

$$h'[n]=C_M[n-k_0]h[n-L] \tag{14}$$

By definition, we have

$$H'(z)=\sum_{n=L}^{L+N-1} C_M[n-k_0]h[n-L]z^{-n} \tag{15}$$

From (10), we have

$$H'(z)=z^{-k_0}\sum_{i=n_0}^{n_1} h[iM+k_0-L]z^{-iM} \tag{16}$$

where

$$n_0=\left\lceil\frac{L-k_0}{M}\right\rceil \text{ et } n_1=\left\lfloor\frac{L-k_0+N-1}{M}\right\rfloor \tag{17}$$

If H(z) is restricted such that

$$h[n]=\begin{cases}(-1)^L & \text{when } n=k_0+i_0M\\ 0 & \text{when } n=k_0+iM \text{ and } n_0\leq i\neq i_0\leq n_1\end{cases} \tag{18}$$

then we obtain $H'(z)=z^{-k_0-i_0M}$ or

$$w[n] = x[n-k_0-i_0M]. \tag{19}$$

So the overall signal component is just a delayed version of the input sequence. The coefficient not specified by (18) have no effect on the overall signal component, so they may be chosen to minimize the overall quantization error component.

3.2. Overall quantization error component and non-ideal error component

The meaningful of the overall quantization error component is it power which can be written as

$$P_e=\frac{1}{2\pi}\int_{-\pi}^{\pi} S_{ee}(e^{j\omega})d\omega\,, \tag{20}$$

where $S_{ee}(e^{j\omega})$ is the power spectral density of the overall quantization error component. To evaluate (20), it is necessary to calculate $S_{ee}(e^{j\omega})$. From (4), it follows that

$$e_q[n]=\sum_{i=0}^{M-1} u_i[n-k_0]e_i[n] \tag{21}$$

where $e_i[n]=e_{qi}[n]*h[n]$ is the quantization error contributed by the i-th ΔΣ modulator as measured at the output of the channel filter. The autocorrelation of $e[n]$ is defined as $R_{ee}[k]$ = E[e[n]e[n+k]]. Substituting (21) into this definition and interchanging the expectation and the

summation results in

$$R_{ee}[k]=\sum_{i=0}^{M-1}\sum_{j=0}^{M-1}u_i[n-k_0]u_j[n-k_0+k]\mathrm{E}\left(e_i[n]e_j[n+k]\right) \quad (22)$$

Because $e_i[n]$ and $e_j[n+k]$ are uncorrelated and $R_{eiei}[k]$, the autocorrelation of $e_i[n]$ is independent of i, for many of the known ΔΣ modulators and the most practical input signal that do not overload the ΔΣ modulators [3]. It follows that (22) reduces to

$$R_{ee}[k]=C_M[k]R_{eiei}[k]. \quad (23)$$

where $C_M[k]$ is defined in (10) which is a well-known sequence in the field of multirate signal processing and is called the comb sequence.

Taking the Fourier transform of (23) using the comb sequence modulation formula derived in [5] results in

$$S_{ee}(e^{j\omega})=\frac{1}{M}\sum_{k=0}^{M-1}s_{eiei}\left(e^{j(\omega-2\pi k/M)}\right) \quad (24)$$

The quantization error component $e_i[n]$ contributed by the i-th ΔΣ modulator is usually considered as additive uniformly distributed white noise source [3]. Applying this method gives

$$S_{eiei}(e^{j\omega})=\frac{\Delta^2}{12}\left|N(e^{j\omega})H(e^{j\omega})\right|^2 \quad (25)$$

where $N(z)$ is the effective filter imposed on the white quantization noise by the ΔΣ modulators, and Δ is the quantization step size. Thus, the power spectral density of the overall quantization error component can be written as

$$S_{ee}(e^{j\omega})=\frac{\Delta^2}{12M}\sum_{k=0}^{M-1}\left|N(e^{j(\omega-2\pi k/M)})H(e^{j(\omega-2\pi k/M)})\right|^2 \quad (26)$$

Combining (20) and (26) gives

$$P_e=\frac{1}{2\pi}\int_{-\pi}^{\pi}\frac{\Delta^2}{12M}\sum_{k=0}^{M-1}\left|N(e^{j(\omega-2\pi k/M)})H(e^{j(\omega-2\pi k/M)})\right|^2 d\omega \quad (27)$$

Since the discrete-time Fourier transform are periodic-2π, this expression can be written as

$$P_e=\frac{\Delta^2}{24\pi}\int_{-\pi}^{\pi}\left|N(e^{j\omega})H(e^{j\omega})\right|^2 d\omega \quad (28)$$

From this expression, we can calculate the power of the overall quantization error component versus the modulator order, the channel number and the channel filter. As presented in [6], the optimal filter can be determined under constraints (18) so that the overall quantization noise is minimized. In this case the theoretical performance can be calculated. The change from low-pass modulators to high-pass modulator retains an interesting property of this architecture that is 6L dB of gain for the overall performance when the channel number is doubled. However it is not it's main advantage which is the possibility to minimize the effects of channel mismatch being the characteristic problem of parallel architecture.

In effect, the non-ideal error component contains 2 components mainly, one from channel gain mismatch and another from offset mismatch which is a low frequency noise. The effect of channel gain mismatch may be minimized thanks to digital equalization technique which was analyzed in [2]. In the other hand, the low frequency noise is emerged completely in the quantization noise. Because the quantization noise introduced by the high-pass ΔΣ modulator differently from the case where conventional ΔΣ modulator is used, is shaped to low frequency region. Let's $E_{ni}\left(e^{j\omega}\right)$ the power spectral density of the low frequency noise of the i-th channel. The noise component in the channel filter output can be written as

$$S_{noise}\left(e^{j\omega}\right)=\left(\frac{\Delta^2}{12}\left|N(e^{j\omega})\right|^2+\left|E_{ni}\left(e^{j\omega}\right)\right|^2\right)\left|H(e^{j\omega})\right|^2 \quad (29)$$

Because the channel filter H(z) is a high-pass filter, the effect of the low frequency noise is removed completely by the channel filter. The level of the quantization and low frequency noises is attenuated as the desired level. This explains the absence of the undesired tones generated by low frequency noise in the spectrum of the overall output signal.

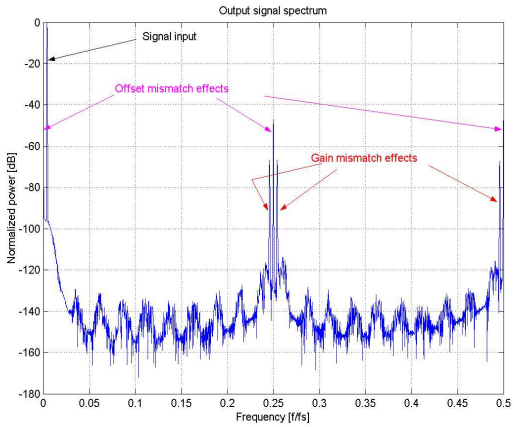

Figure 3. Output spectrum of TI ΔΣ ADC with 4 channels

The figure 3 shows clearly the effects of the channel mismatch in the conventional TI ΔΣ converter, especially the channel gain mismatch and offset mismatch. The overall non-ideal error component is the sum of the channel non-ideal error component after taking a down-sampling and an interpolation as indicated in (4). After these two operations, as indicates in (26), the quantization noise introduced by the i-th channel is a scaled copy of the one introduced by the first channel. This phenomena will happen also with non-ideal error component. That's why the offset mismatch causes M undesired tones at causes additive tones at integer multiples of F_s/M and channel gain mismatch results in input samples amplitude modulation, causing input spectrum scaled copies to appear centered around integer multiples of F_s/M.

As shown in the figure 4, the effects of the offset

mismatch is completely removed. Since the low frequency noise is emerged in the quantization noise, the overall noise in each channel is removed by the high-pass channel filter. We showed also in [2] that the use of high-pass modulators does not affect the problem caused by the channel gain mismatch, but allows simple but efficient digital correction method which does not work very well in presence of channel offsets.

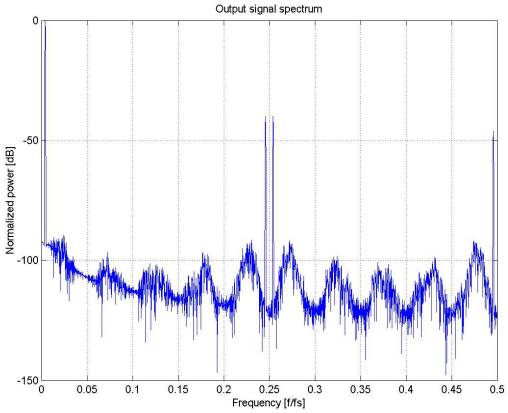

Figure 4. Output signal spectrum of the TI high-pass ΔΣ ADC

4. ADAPTIVE GAIN EQUALIZATION

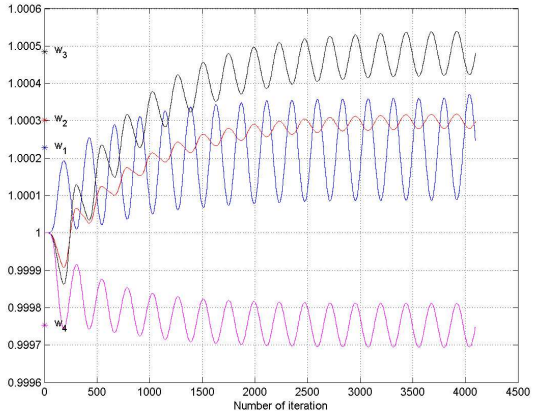

Figure 5. Magnitude of the weights as they oscillate around the desired values

The channel gain mismatch could be equalized simply by adding an extra multiplier after each channel output. Each channel gain is multiplied by a weight. When the weights are chosen to be the inverse of the respective channel gain, the overall channel gain will be unity, and the effects of the channel gain mismatches will be removed. We have proposed a simple adaptive scheme based on the well known least-mean-square (LMS) algorithm thanks to its implementation simplicity [2]. For even greater implementation simplicity, the sign-data, the sign-error and the sign-sign LMS (SD-LSM, SE-LMS and SS-LMS respectively) algorithms are proposed and studied also [2]. The comparison of theses 4 algorithms results that the SD-LMS algorithm is the best in term of simplicity implementation and performance [2]. This method seems like very simple and efficient. A question can be asked here is whether it can be applied to the conventional TI ΔΣ converter. We will analyze this problem and then clarify the role played by high-pass modulators. In presence of the offset, LMS algorithm does not converse, instead of convergence, the weighs oscillate around the desired values as shown in the figure 5. Consequently the effects of channel mismatch is not really minimized.

We showed in [2] that in absence of offsets, the adaptive gain equalization used is very efficient. The effects of channel gain mismatch can be almost eliminated. In presence of the offsets, it is difficult to equalize channel gains. From which we conclude another advantages of high-pass ΔΣ modulators .

5. CONCLUSION

A TI high-pass ΔΣ ADC architecture has been introduced and analyzed. The high-pass ΔΣ modulator moves the quantization noise to low frequency region. So the low frequency noise is emerged in the quantization noise. Consequently, these noise are filtered by the channel high-pass filter. Another advantage of the high-pass modulators is that they allow a simple but efficient gain equalization technique to minimize the effects of channel gain mismatch. The simulation gives a good result but additional work is necessary to implement a test circuit and establish the limitation of the approach.

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6. REFERENCES

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