A DVD PROCESSOR WITH DUAL CPUS AND INTEGRATED DIGITAL FRONT-END FOR ADVANCED DVD-BASED CONSUMER APPLIANCES

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1. ABSTRACT

We present a single-chip DVD processor. It combines two 32-b RISC cores, a 24-b/32-b audio DSP, video MPEG and subpicture decoders, a graphics and video processor with six video DACs that supports both progressive and interlaced output video, audio, video, and I/O interface units, and several dedicated processing units. In addition, the processor integrates the front-end channel decoder and error correction functions, traditionally part of the DVD loader circuitry. The DVD processor has been implemented using a standard-cell library in 0.18 μm CMOS technology.

2. INTRODUCTION

Few consumer electronic products can match the recent success and growth of DVD players. At the core of each DVD player is a single-chip DVD decoder IC that usually integrates a CPU core for overall control and navigation, an MPEG video decoder, a DSP for audio decoding, and I/O interfaces for peripheral devices, such as the DVD loader, the NTSC/PAL video encoder, and front-panel control. The latest generation of DVD decoder ICs[1, 2, 3] may also provide enhanced features such as virtual surround audio, DVD-Audio, integrated video DACs and progressive video output.

The wide acceptance of the DVD format combined with the introduction of integrated audio-video MPEG-2 encoders[4] lend to the introduction of a new generation of consumer products that combine DVD playback with other functions, such as audio juke boxes or digital video recording. Examples include: DVD recorders, personal video recorders with DVD playback, or home media centers[5]. These new products require additional processing power to accommodate new applications, such as video editing, managing audio and video libraries, and video streaming. In this paper we describe the architecture of an advanced DVD processor, the CS98200, which is ideally suited for such applications. It integrates two 32-b CPUs, a 24-b/32-b audio DSP, video MPEG and subpicture decoders (with a special co-processor for MPEG-4 decoding), and several other dedicated units, including a video encoder with six video DACs.

The CS98200 integrates also the digital front-end channel decoder, traditionally part of the circuitry in the DVD drive. Using a separate mixed-signal front-end IC, the CS98200 can interface directly with the optical pickup unit (OPU) of a DVD loader. The computational power of the CS98200, combined with a rich set of peripheral I/O functions make it ideal for the design of DVD-based consumer appliances. An example design of a DVD recorder system is presented.

3. SYSTEM ARCHITECTURE

Figure 1 shows a simplified block diagram of the CS98200 DVD processor. It includes two 32-b RISC processors (RISC0

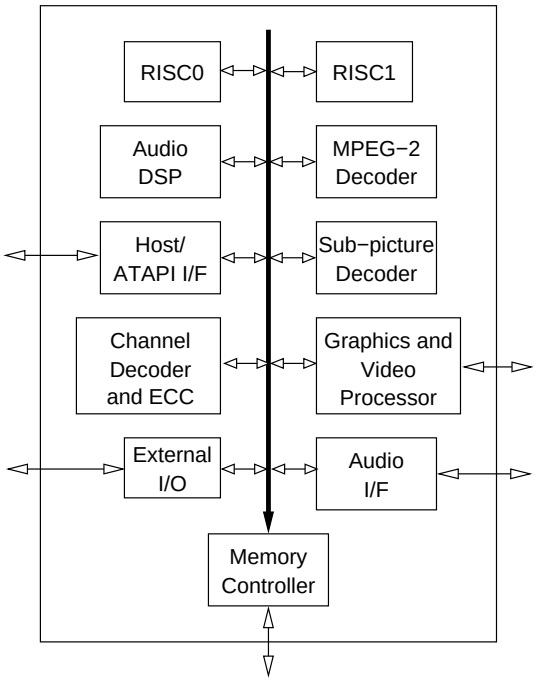

Fig. 1. Block diagram of the CS98200 DVD processor.

and RISC1), an audio DSP, a video MPEG decoder, a DVD subpicture decoder, a serial DVD loader I/O, host/ATAPI interface, simple I/O interfaces, a video capture interface, memory controller, graphics and video processors, NTSC/PAL video encoder, and front-end channel decoder. Given an input 27 MHz clock, internal PLLs generate all required clocks for the RISC processors and the DSP (180 MHz), memory (up to 120 MHz), and the rest of the processor (81 MHz).

3.1. The RISC Processors

The CS98200 includes two proprietary 32-b RISC processors, RISC0 and RISC1. RISC0 is used mostly for real-time control of low-level system functions. In addition, RISC0 coordinates on-chip multi-threaded tasks and the front-panel and remote control operations.

RISC1 is used for user-level applications and control. RISC1 can access system resources controlled by RISC0 using calls through an applications programming interface (API). Both processors are fully programmable with support for C compilers and debuggers and real-time operating systems.

3.2. The Audio DSP

This is a proprietary, programmable, DSP, optimized for audio applications. It performs 24-b fractional operations and 32-b integer and logic operations, with a 54-b accumulator. A built-in multiplier-accumulator has single-cycle throughput with a two-cycle latency. Dedicated hardware allows for efficient bit parsing and unpacking operations. The DSP supports all popular audio formats, including MPEG audio (all Layers), Dolby Digital or DTS (6 channels), and DVD-Audio (8 channels).

3.3. MPEG Video and Subpicture Decoder

For MPEG-1 and MPEG-2 bit streams, video decoding is performed using dedicated hardware. For MPEG-4 and other codecs, video decoding is performed using both the RISC0 processor and dedicated hardware. For example, for MPEG-4, RISC0 performs bit-stream handling, variable length decoding, and inverse quantization. Special hardware controls coefficient saturation, the inverse DCT, and motion compensation. The video decoder processes I, B, and P frames, and writes to the video frame buffers in DRAM for output to the display. It supports all popular video formats, including VCD, SVCD, DVD, and MPEG-4 simple profile[4]. A subpicture decoder includes a hardware-based run-length decoder for DVD sub-pictures[6], hardware-based vertical scaling for NTSC-PAL conversions, and supports 16-level alpha blending.

3.4. Memory Controller

The memory controller provides all interface and arbitration functions between the CS98200 modules and external memory, such as SDRAM, Flash, or ROM. Using a 32-b memory interface, it supports up to 32 Mbytes of external SDRAM. An internal DMA controller can be used for a more efficient transfer of data between external SDRAM and internal memory. A special block-DMA call allows transfers of data from one block of external memory to another block of external memory. This feature combines a DMA read and a DMA write into one operation.

3.5. Video and Graphics Processing

The CS98200 integrates an NTSC/PAL video encoder with six 10-b video DACs. These DACs provide two S-Video output channels, one composite video output, and three R, G, B, or Y, Pb, and Pr component outputs. Video output can be either interlaced (NTSC or PAL) or progressive and it is compliant with Macrovision protection.

A separate digital video input port allows the processor to be connected directly to video decoders using either the ITU-R 656 or the ITU-R 601 interfaces, in both master or slave modes. This is a unique feature for a DVD decoder IC and allows the CS98200 to be used in systems with multiple video sources, such as DVD recorders.

The video processor allows for the scaling and overlay of multiple video planes (main video, video input, picture-in-picture, and on screen display). A simplified block diagram of the video multiplexing and overlays is shown in Figure 2.

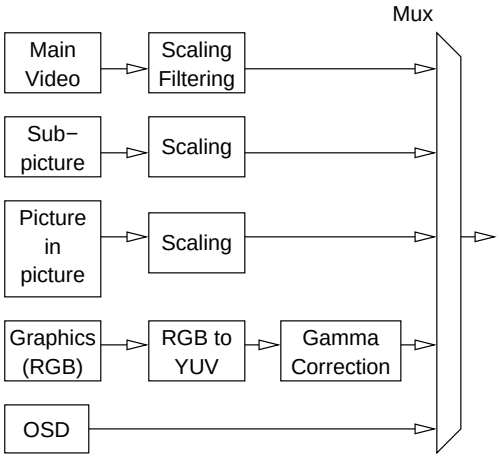

Fig. 2. Video multiplexing on the CS98200 processor.

3.6. System Interfaces

In addition to the main DVD processor, a DVD-based system will usually include a number of other peripheral devices, such as a video decoder, audio ADs and DAs, and a DVD drive. The CS98200 integrates a number of system interfaces for glue-less connection to peripheral devices. These interfaces include: a generic 16-b or ATAPI host interface, I^2C, UART, and SPI interfaces for inter-chip communication, I^2S, AC97, and S/PDIF audio interfaces, and a separate DVD-loader serial interface. In addition, the CS98200 provides a unique digital front-end loader interface, which is examined in more detail in the next section.

4. DIGITAL FRONT-END LOADER INTERFACE

In most DVD players, the DVD controller (usually called the front-end) is part of the circuitry in the DVD drive. The DVD controller can be divided into two parts: a mixed-signal front-end and the digital DVD/CD channel decoder. The mixed-signal front-end includes such components as: the pickup-interface, the servo interface, a servo controller, a digital or analog read channel, and a clock synthesizer. The channel decoder includes: a DVD/CD Frame detector, EFM/EFMP demodulation, error correction, descrambler, buffer streamer, a host/ATAPI interface, SDRAM interface, a DVD authentication module, and an audio DAC interface for PC applications.

By removing duplicate circuitry, such as the SDRAM controller and ATAPI interfaces, which are already part of the CS98200, we were able to integrate the complete channel decoder into the CS98200 and provide a more cost-effective solution for DVD players. Figure 3 shows a block diagram of the circuitry in the channel decoder. In DVD mode, NRZ data are multiplexed between data from the information area and the burst cut area (BCA) of the loader. Captured data are first decoded and assembled as ECC blocks in the SDRAM. The data is then corrected and descrambled by the ECC and descrambler blocks and is transferred to the Track Buffer area in SDRAM so that they can be demultiplexed and decoded.

In CD mode, the device accepts NRZ data from the loader and performs demodulation, de-interleaving, C1/C2 correction, and sub-code processing. Then, the data is assembled as sectors in SDRAM for further processing, depending on the data type; for example, CD-DA, MP3, VCD, and SVCD.

Figure 4 shows a typical connection of a DVD drive with a mixed-signal front-end IC and the CS98200. The DVD drive includes only the drive mechanism and the optical pickup unit (OPU). The mixed-signal, front-end, chip sends NRZ data through the decoder I/O bus in the CS98200. Communication and control can be performed using either the ATAPI/host interface bus or the DVD serial bus.

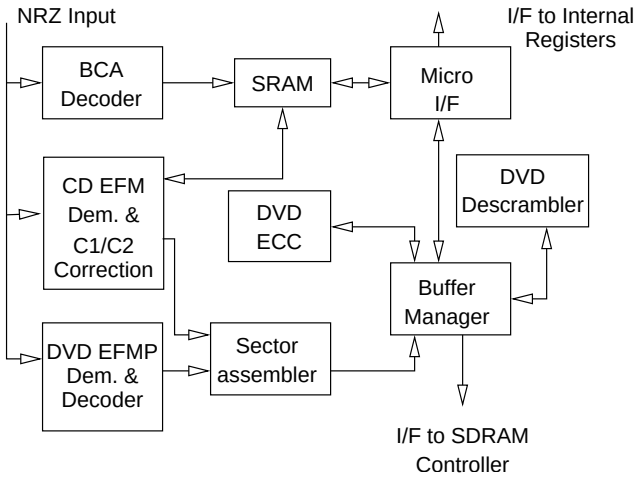

Fig. 3. Front-end channel decoder.

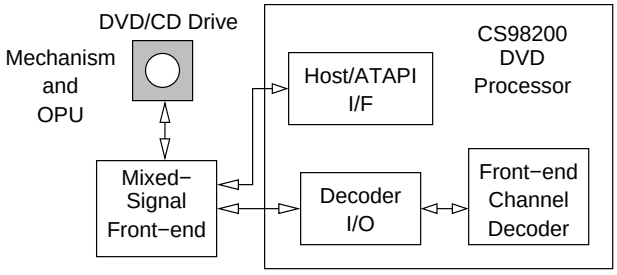

Fig. 4. Typical connection of the CS98200 with DVD mechanism and OPU.

5. SOFTWARE ARCHITECTURE

Figure 5 shows a simplified view of the software architecture for the RISC0 and RISC1 processors. Grayed-out blocks can be developed either internally or by software partners and customers. The rest of the blocks are usually developed internally. As mentioned before, both processors intercommunicate using an inter-processor-communication (IPC) API.

At the bottom layer of the software architecture are chip drivers. These control the operation of the internal hardware components of the CS98200, like the video processor, the DSP, and the I/O peripherals. A real-time operating system can run on either both the RISC processors or just RISC0. At this point, the CS98200 supports the Nucleus RTOS[7]; however, other operating systems could be supported as well.

Software for external drivers includes libraries for DVD loaders, IDE drives, networking, and other external peripherals. Middleware refers to software libraries that reside between the applications and the external device drivers. Examples include: the DVD navigator, electronic program guides, databases for personal video recorders, and interac-

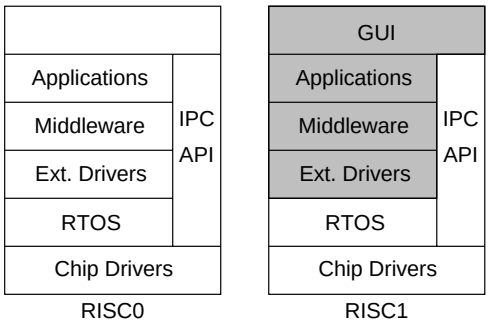

Fig. 5. Software architecture for RISC0 and RISC1

tive DVD or Web services.

The application layer includes such applications as: disc player (such as DVD and audio CD), personal video recorder, DVD recorder, and audio/video juke boxes. Finally, at the top of the software architecture we have the graphical user interface; that is, the menus that help users interact with the applications.

6. SYSTEM DESIGN EXAMPLE

As an example system design, Figure 6 shows a block diagram of a digital video recorder using the CS98200 DVD processor and an MPEG-2 encoder. In this example, the

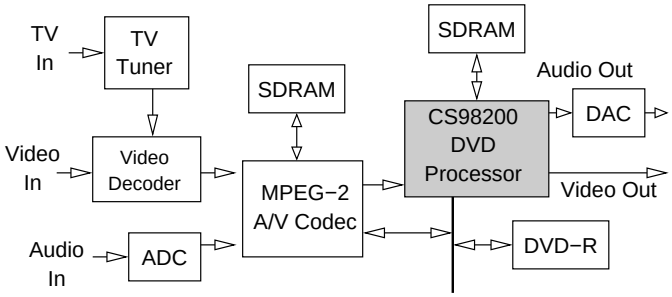

Fig. 6. System design for a DVD recorder.

host/ATAPI bus is used both as an IDE/ATAPI bus to communicate with an IDE-based DVD-recordable drive and as a generic bus to communicate with the MPEG encoder. All the application software for the DVD recorder runs on the CS98200. Examples of high-level functions include: scheduling recordings using the external TV tuner, managing prerecorded material (list, edit, delete), or DVD, Photo CD, and audio CD playback.

During encoding, digital audio and video are captured by the MPEG encoder, compressed, and multiplexed into an MPEG program stream. The compressed bit stream is transferred using DMA reads and writes from the MPEG encoder's SDRAM into the CS98200 SDRAM. The compressed bit stream is further processed according to the DVD format, and a DVD-compliant stream is written into the DVD recordable drive.

For digital video loopback, the input video can be passed through to the CS98200 using its video input capture port. There, it can be mixed and overlayed with on-screen-data (OSD), for example, for menu control. During playback, data from the DVD drive are transferred to the CS98200 where they are decoded and played back.

7. STATUS AND CONCLUSIONS

In this paper we presented the architecture of an advanced DVD processor. The chip was designed by taking into consideration the processing and interface requirements of a new generation of consumer appliances that combine DVD playback with advanced functions, such as Web interaction, audio receivers, and audio juke boxes. Combined with an MPEG encoder, it can provide full-duplex DVD playback and recording functionality for time-shift or DVD-recordable applications. The CS98200 DVD processor has been implemented using a standard-cell library in 0.18 μm CMOS technology.

8. ACKNOWLEDGMENTS

We would like to thank all the hardware and firmware engineers that have contributed to the design and implementation of this processor.

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