DIGITAL TIMING SYNCHRONIZATION WITH JITTER REDUCTION TECHNIQUE FOR CAP-BASED VDSL SYSTEM

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ABSTRACT

This paper describes a digital timing synchronization method for the CAP-based VDSL system. An adaptive loop filter with digitally controlled loop gain is proposed for jitter performance improvement. The proposed loop filter allows both fast locking and low steady state jitter. A digital spectral line method is used for robust timing extraction. Simulation results show that RMS timing jitter is less than 0.4% of the symbol period even for the worst case channel and synchronization is established within 400 symbol periods. The VDSL system is implemented in a 0.6μm CMOS technology, and tested. The measured peak-to-peak timing jitter is about 0.1% of the symbol period, which makes the VDSL system receive data up to 52Mbps over the telephone wire.

I. INTRODUCTION

Very-high-speed digital subscriber line (VDSL) system has been developed to provide high-speed data transmission services on an unshielded twisted pair (UTP) copper wire [1]. Since the transmission channel of the UTP category 3 (UTP-3) shows very poor frequency characteristics for high-speed signals with the bit rate up to 52Mbps and the symbol rate up to 13Mbaud, line code has been carefully chosen in order to overcome the channel degradation and impairments. The discrete multi-tone (DMT) line code supported by VDSL Alliance, one of the VDSL standardization groups, provides one of the solutions for transmitting high-speed data over UTP-3. With the multi-carrier modulation approach, it can fully use available channel capacity and improve overall modem performance, but requires complex hardware. Alternatively, the carrierless amplitude and phase modulation (CAP) line code [2] can be chosen along with well-established modulation methods such as quadrature amplitude modulation (QAM), and require less complex hardware, compared with DMT-based modem. Because of the hardware simplicity, VDSL Coalition, the other VDSL standardization group, chooses the CAP/QAM line code for its modulation method. However, the CAP-based modem requires an elaborate symbol timing synchronization block that could significantly affect overall performance and then restrict the maximum data rate to transmit. Since the overall demodulator performance is sensitive to symbol timing offset and jitter, the exact and stable acquisition of the symbol timing is important to guarantee the quality of the VDSL service. Moreover, since several noisy sources exist and the channel distortion is serious, the timing synchronization should be insensitive to such impairments.

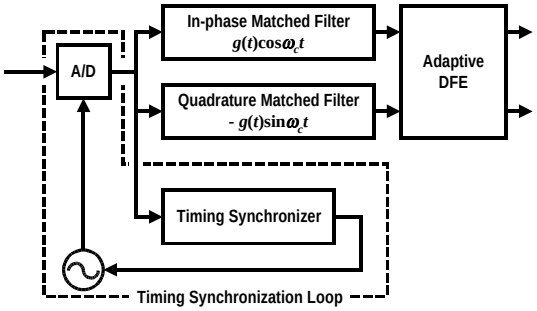
For the robust timing synchronization, a digital spectral line method was proposed for 16-CAP VDSL system [3]. It needs less complex hardware for implementation, compared with the conventional spectral line method. However, the jitter performance is degraded exponentially, as channel length increases, because of serious channel distortion. The jitter performance is related with the loop bandwidth [4]. Therefore, the optimization of the timing loop bandwidth is necessary to overcome such degradation. The gear-shifting algorithm gives optimal solution [5], but requires somewhat complex hardware. To simplify hardware, a heuristic jitter reduction method has been developed [6]. It exploits a simple loop gain adaptation scheme.

This paper presents a digital timing synchronization method with the jitter reduction technique for the CAP-based VDSL system. It is verified with computer simulations and VLSI implementation. In section II, the general receiver architecture is briefly described, and the digital spectral line timing synchronization method is also reviewed. An adaptive loop filter for the jitter performance improvement is introduced in section III. Section IV provides the simulated and measured results. Finally, section V draws conclusion.

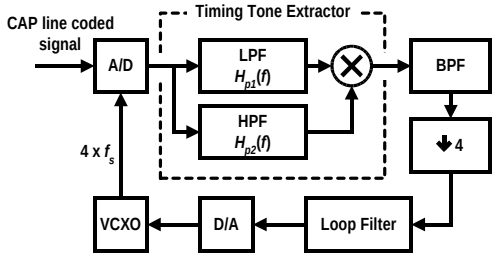
II. ARCHITECTURE OVERVIEW

Fig. 1-(a) shows the general receiver architecture for the CAP-based VDSL system. With the timing synchronization loop, the received signal is sampled in an analog-to-digital converter and demodulated in in-phase and quadrature matched filters. The adaptive decision feedback equalizer (DFE) follows in order to compensate for the channel distortion. The timing synchronization loop, which adopts the digital spectral line method [3], is shown in Fig. 1-(b).

The timing tone is extracted through two pre-filters and one multiplier. The received CAP signal $s(t)$ is band-limited



(a) Receiver architecture



(b) Digital spectral line timing synchronization

Fig. 1. CAP-based VDSL receiver

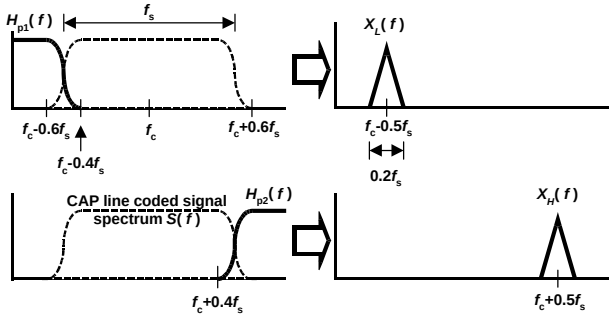


Fig. 2. Pre-filtering on received signal

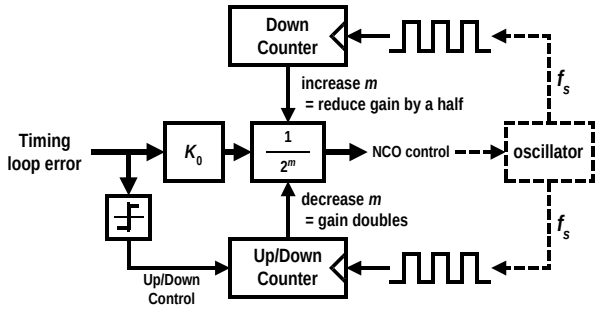


Fig. 3. An adaptive loop filter with digitally controlled loop gain

to [f_c–0.6f_s , f_c+0.6f_s], where f_s is the symbol rate and f_c is the center frequency. As shown in Fig. 2, the pre-filter $H_{p1}(f)$ is a low-pass filter which extracts lower edge of the signal spectrum and the other pre-filter $H_{p2}(f)$ is a high-pass filter which extracts higher edge. When sampled with 4f_s clock, the low-passed signal can be represented as

$$x_L(n) = s(n) * h_{p1}(n) \cong x(n)\cos(2\pi(f_c - 0.5f_s)n/4f_s) \quad (1)$$

where $x(n)$ is the sampled version of the band-limited signal $x(t)$ in [–0.1f_s, 0.1f_s]. In case of the high-passed signal,

$$x_H(n) = s(n) * h_{p2}(n) \cong x'(n)\cos(2\pi(f_c + 0.5f_s)n/4f_s) \quad (2)$$

where $x'(n)$ is a band-limited signal similar to $x(n)$. Since these filtered signals are apart by f_s in the frequency domain, the timing tone at f_s, corresponding to (f_c+0.5f_s)–(f_c–0.5f_s), can be obtained through multiplication of these filtered signals. The band-pass filter is used to improve the spectral purity of the timing tone and eliminate the other spectral tone, corresponding to (f_c+0.5f_s)+(f_c–0.5f_s), generated from the timing tone extractor. The band-pass filter finally produces the sampled sinusoidal waveform with frequency of f_s, which consists of 4 samples per symbol period. The band-passed signal is thereby decimated by a factor of 4. The decimated signal controls an external voltage controlled crystal oscillator (VCXO) generating the sampling clock so that, when adjusted, the timing error becomes 0.

II. LOOP FILTER DESIGN

Additive white noise and data pattern dependent noise create jitter in the timing signal. In order to reduce the jitter created from such noise, the loop bandwidth optimization becomes necessary. Since the loop bandwidth is directly related with the loop gain [4], it can be optimized with the loop gain optimization.

A. Loop gain optimization

The timing synchronization loop in Fig. 1-(b) can be simply modeled as the 1st order loop given by

$$\tau(k+1) = \tau(k) - G(k)e(k) \quad (3)$$

where $G(k)$ and $e(k)$ is the loop gain and timing error at time k, respectively. The timing error is divided into the conditional mean of $e(k)$

$$\tilde{e}(\tau(k)) = E\{e(k) \mid \tau(k)\} \quad (4)$$

and an additive noise $N(k)$ with a zero mean, and then (3) is rewritten as

$$\tau(k+1) = \tau(k) - G(k)\{\tilde{e}(\tau(k)) + N(k)\} \quad (5)$$

Since the timing error is monotonically increased near the optimal timing τ_{op}, the linear approximation on $\tilde{e}(\tau(k))$ is

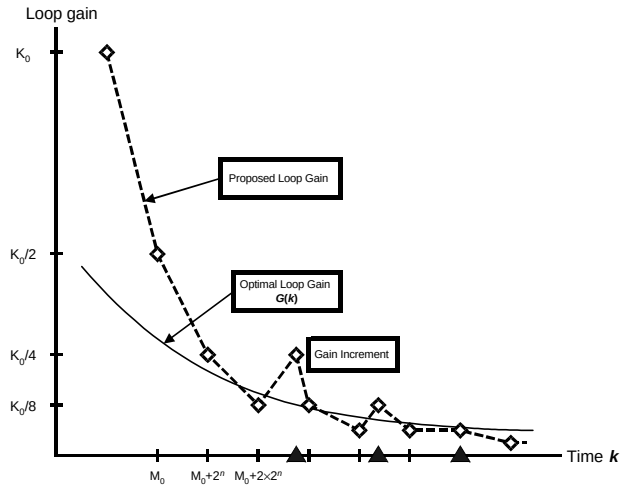


Fig. 4. Loop gain adaptation to approximate the optimal loop gain $G(k)$

possible. With linearization, the timing loop equation finally becomes

$$\tau(k+1) = \tau(k) - \gamma G(k)\{\tau(k) - \tau_{op} + N(k)/\gamma\} \qquad (6)$$

where γ is the slope at τ_{op}. Referring to [5], the optimal loop gain in this case is given by

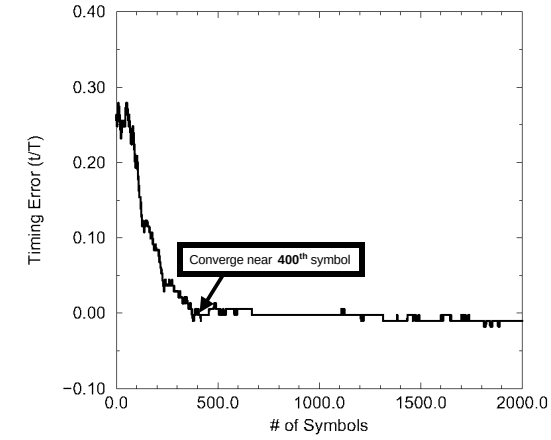
$$G(k) = \frac{1}{\gamma}\frac{1}{k+1} \qquad (7)$$

for the minimum mean squared error (MMSE) criterion. It needs a true multiplier for implementation, and $1/\gamma$ should be estimated. Therefore, a heuristic design, which provides loop gain close to the optimal given by (7) and is implemented with only shifters and adders, is preferred.

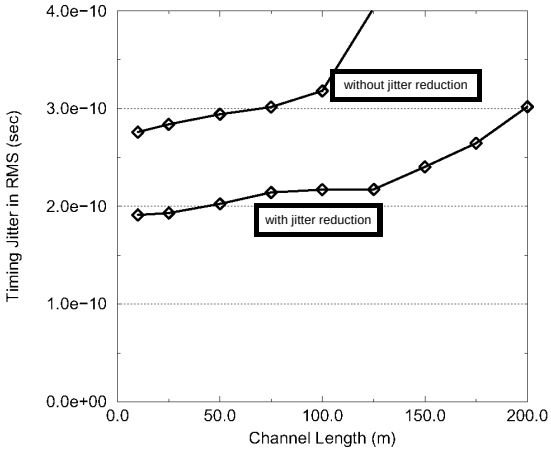
B. Proposed adaptive loop filter design

Fig. 3 shows a digitally controlled loop filter of which the gain varies from a fixed gain K_0 to a controlled gain $K_0 \times 1/2^m$, where m is a nonnegative integer. K_0 is not related with $1/\gamma$, and then can be chosen arbitrarily. Normally, K_0 is set to 1 in order to simplify the implementation.

Two counters, while clocked with symbol rate, separately control the variable m. The first n-bit down counter generates a control signal to increase m by 1 when the counter becomes 0 and decreases the loop bandwidth accordingly. The second n-bit up/down counter generates another control signal to decrease m by 1 when the counter becomes either 2^n-1 or 0 and increases loop bandwidth accordingly. The n-bit up/down counter behaves as an up counter if the timing error is positive, or as a down counter if the timing error is negative. The up/down counter is initially set to 2^{n-1}. When the counter becomes 0 or 2^n-1, it is reset to 2^{n-1}.



(a) Convergence of timing extraction



(b) Simulated timing jitter performance

Fig. 5. Simulation results

When the recovered timing phase is far off the optimal, timing error becomes either consecutively positive or negative, statistically. In this case, the up/down counter keeps either increasing or decreasing depending on the sign of the timing error and increases the loop gain. Therefore, faster locking is possible. On the other hand, when the timing phase is near optimal, the timing error alternates between positive and negative values. In this case, the up/down counter stays around its initial value, and the loop gain gradually reduces according to the control signal from the down counter. With this control scheme, the optimal loop gain given by (7) can be approximated as shown in Fig. 4. Therefore, the efficient loop bandwidth control is possible and both fast locking and low steady state jitter are allowed.

IV. SIMULATED AND MEASURED RESULTS

For the computer simulation, the transmission channel of UTP-3 is modeled as described in [1]. The propagation loss

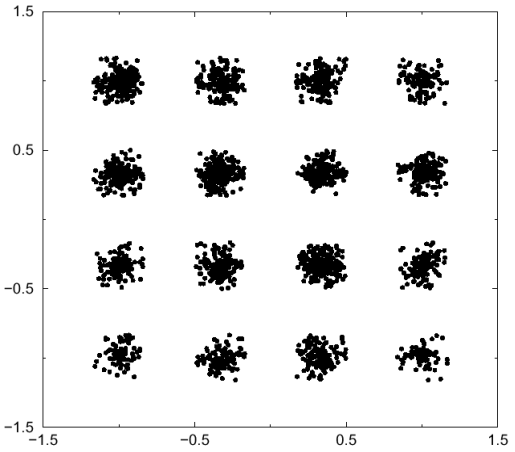


Fig. 6. Reconstructed 16-CAP constellation

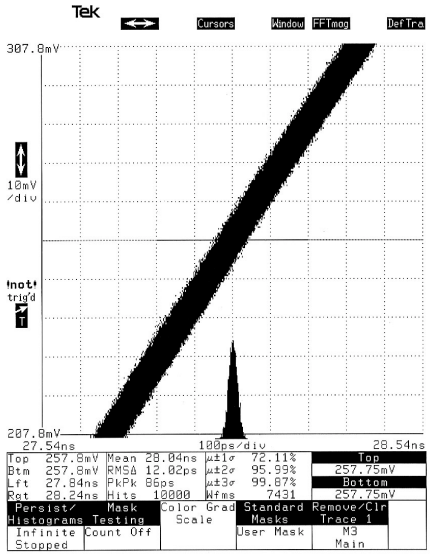


Fig. 7. Jitter histogram at symbol rate of 10Mbaud

and phase delay are modeled by referring to [7][8]. Also, some channel impairments such as additive white Gaussian noise (AWGN) and crosstalks are considered.

The transmission profile with the symbol rate of 12.96Mbaud is simulated. Fig. 5-(a) shows the timing extraction with the proposed jitter reduction technique. The simulated locking time is less than 400 symbol periods for 200m UTP-3 channel. Fig. 5-(b) shows the timing jitter performance for the channel length. The simulated timing jitter is within 0.4% of the symbol period in RMS.

The VDSL system with the proposed timing synchronization method is implemented in a 0.6μm CMOS technology. The measured 16-CAP constellation, which is reconstructed by the adaptive DFE, is shown in Fig. 6. The soft decisions are clustered about the hard-decision points with the signal-to-noise ratio (SNR) of 18dB, which provides bit error rates (BER) of about 10^{-7}, for 200m UTP-3 channel. As shown in Fig. 7, the measured cycle-to-cycle timing jitter is 12.02psec in RMS and 86psec in peak-to-peak at the symbol rate of 10Mbaud. Equivalently, the measured peak-to-peak timing jitter is less than 0.1% of the symbol period.

V. CONCLUSION

The digital timing synchronization with the jitter reduction technique is presented. It is employed in the CAP-based VDSL system. For the jitter performance improvement, the adaptive loop filter with digitally controlled loop gain is proposed, and it achieves both fast locking and low steady state jitter. The proposed synchronization method provides the exact and stable symbol timing enough to guarantee the quality of the VDSL service.

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