A SINGLE-CHIP MPEG-2 MP@ML AUDIO/VIDEO ENCODER/DECODER WITH A PROGRAMMABLE VIDEO INTERFACE UNIT

C.T. Chen, T.C. Chen, F-C. Jeng, H. Cheng, K. Konstantinides

Stream Machine
San Jose, CA
USA

1. ABSTRACT

We present a single-chip, MPEG-2 Main Profile at Main Level, audio and video encoder and decoder. It combines a RISC core, a 24-bit DSP, video and audio interface units, and several dedicated processing units. A programmable video interface unit supports multiple modes of pre- and post-processing and on-screen display (OSD). The codec has been implemented using a standard-cell library in 0.18 μm CMOS technology.

2. INTRODUCTION

The adoption of the MPEG standard [1] offered consumers a new generation of products, such as DVD players, digital TV, and personal video recorders. While the first generation of MPEG-based products offered playback-only capability, the latest cost effective MPEG-encoding solutions[2, 3] allow for a new class of affordable digital video recording products. These codecs integrate complete MPEG-2 video encoders and decoders; however, a complete digital audio/video system still requires additional hardware for audio encoding and decoding and for multiplexing or demultiplexing the audio and video streams.

In this paper we present an MPEG-2 ML@MP codec that pushes system integration even further, by integrating both audio and video encoding and decoding into a single chip. In addition to real-time audio and video coding, this codec provides programmable support for multiplexing and demultiplexing, pre- and post-processing of video data, and on-screen display (OSD). These combined benefits make this codec an ideal single-chip solution for a variety of MPEG-2-based applications, such as SVCD recorders or USB-based TV/video players and recorders.

3. SYSTEM ARCHITECTURE

Figure 1 shows the major functional units of the MPEG A/V codec. These units include: the RISC microcontroller, the Video Interface Unit (VIO), the Audio Interface Unit (AIU), the Video Engine Unit (VEU), the Audio Engine (DSP), the Host Interface Unit (HIU), and the SDRAM Control Unit (DCU)

All blocks inter-communicate using two major buses: a 64-bit wide data bus (D-Bus) and a 16-bit wide register bus (R-Bus). In addition to the above seven major blocks, the I^2C CTRL block provides control for external NTSC/PAL video encoders and decoders. The PLL block provides clocking for all internal blocks and also external memory. Given an input 27 MHz clock, all internal components operate at 108 MHz. A separate audio PLL is used to provide an output clock for external audio A/D and D/A converters.

3.1. The RISC Microcontroller

This is an embedded, programmable, 32-bit ARC RISC processor [4]. It performs multiplexing of audio and video elementary streams and demultiplexing of MPEG program streams. It also acts as a central controller and sequencer. Its microcode can be downloaded either from an external host or from an external EPROM or Flash memory, through the Host Interface Unit.

The embedded software design effort for such a codec requires code development for two distinct type of tasks: timing-critical tasks, such as video compression, and non-timing-critical tasks, such as multiplexing of audio and video and user communications. One solution for such a system is to use a single RISC processor running a real operating system. In this case context switching time is very important and unless the RISC processor is very powerful it is very difficult to guarantee a predictable behavior for timing critical tasks.

Our solution is different. The RISC core features novel memory mapping and interrupt controlling schemes that allows it to handle both critical timing requirements and traditional software applications, without the need to run a real-time operating system. Specifically, we have dedicated interrupt vectors, and memory (data and instruction) to two

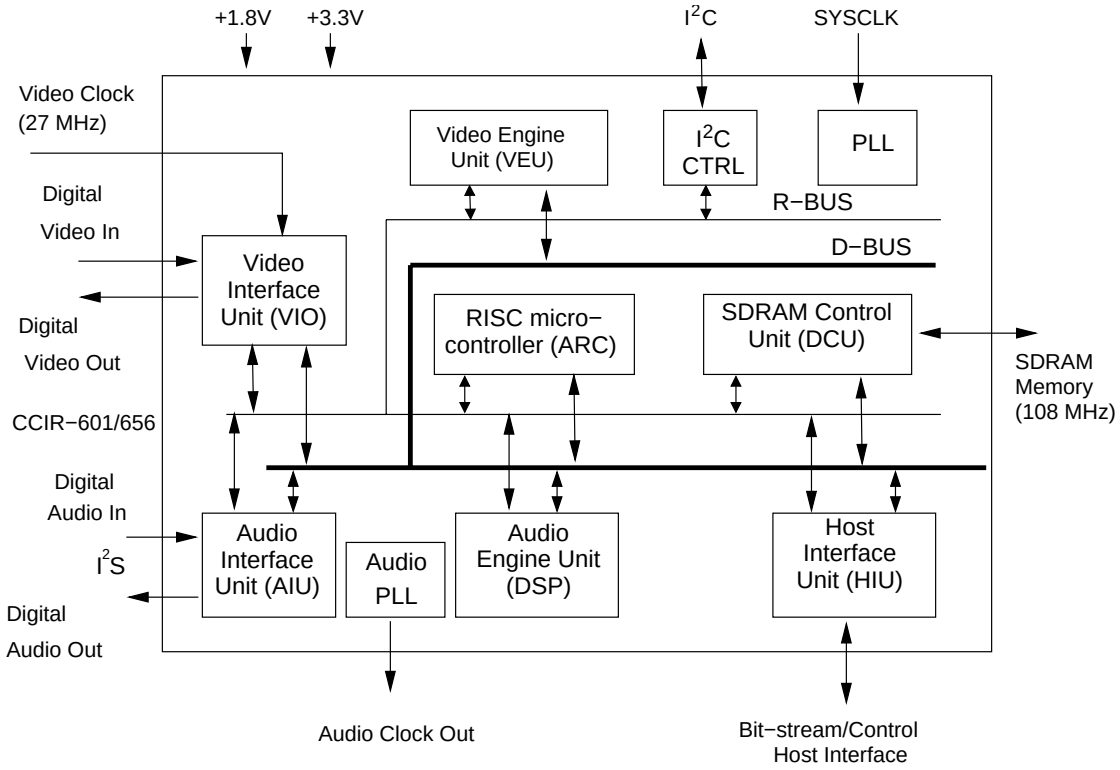

Fig. 1. Block diagram of the MPEG-2 audio/video codec.

different types of tasks: time-critical and non-critical. Since all time-critical tasks are interrupt driven and have their own memory space, there is no need for context switching. This allows for easier software development and predictable performance.

3.2. The Host Interface Unit

The host interface is used to communicate with the host controller and external EPROM or flash memory. It supports a variety of communication protocols, including 16-bit Motorola- or Intel-like interfaces, and a generic 8-bit interface. The host interface has a glue-less interface to USB controllers and it may also be used in PC-based host systems using a PCI bridge interface. The HIU is also used for the I/O of the compressed bit streams between the codec and an external controller.

3.3. The Audio Interface Unit (AIU)

The audio interface unit provides the interface between the codec and external audio devices. Audio samples are transferred in and out of the codec using I^2S signaling. The codec also provides a user-configurable output clock for external audio A/D and D/As.

3.4. The Video Engine Unit (VEU)

Figure 2 shows a block diagram of the VEU. It includes a

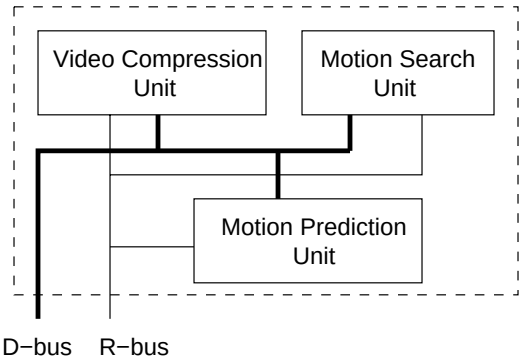

Fig. 2. Block diagram of Video Engine Unit.

video compression unit (VCU), a motion search unit (MSU), and the motion prediction unit (MPU). The VEU is the video processor core for the codec. During encoding, it operates on the video data and generates an MPEG-compliant video elementary stream. Among its many functions, it performs motion estimation and compensation, DCT, quantization, rate control, and variable length coding.

During decoding, it operates on a video elementary stream and generates decompressed video frames. It performs vari-

able length decoding, inverse quantization, IDCT, and motion compensation. The IDCT output is fully compliant with the IEEE-1180 accuracy requirements. A more detailed description of the VEU is given in [2].

3.5. The Audio Engine

The Audio Engine provides the core processing power for all audio-related functions. It consists of an embedded, 24-bit, general purpose, and programmable digital signal processor (DSP). The DSP features a 24 $\times$ 24-bit, multiplier and can perform a multiply-accumulate operation in a single cycle, with no overhead pipeline delay. It features dual data memory banks and a separate program memory. A separate 6-channel DMA engine provides a seamless interface between the external and internal memories and automatic translation from 64 to 24 bits. The Audio engine can support all popular audio formats, such as Dolby Digital and MPEG audio.

3.6. The SDRAM Control Unit (DCU)

The SDRAM control unit (DCU) provides an interface between all functional units and the off-chip memory (SDRAM) storage. It sustains real-time audio and video encoding and decoding at 30 frames per second. The DCU arbitrates the requests from all function units and generates all necessary handshake and control signals for both the requesting unit and the external SDRAM. The data storage boundaries are user-programmable for custom applications. A detailed description of the video interface unit is given next.

4. THE VIDEO INTERFACE UNIT (VIO)

It is well known that the MPEG standard defines only the syntax of an MPEG-compliant stream and the decoding procedure. It leaves quite open the design and implementation of all pre- and post-processing functions, such as filtering, and color downsampling and upsampling. Because of the variety of application in digital video encoding, there is a need for a programmable and flexible video interface unit.

Figure 3 shows a block diagram of the VIO. It includes the Video Input Unit (VIU), the Video Output Unit (VOU), the Video Processing Unit (VPU), and the OSD Unit. The VIU selects the input video active area and performs chroma conversion, inverse telecine, spatial and/or temporal prefiltering, and data arrangement to facilitate the subsequent encoding processes. It preprocesses the input data so that encoding can be done in the most efficient way.

The VOU can perform a variety of postprocessing operations, including horizontal and vertical scaling, telecine, and video format conversion. The OSD block mixes text and/or graphics from the OSD buffer (in SDRAM) with the output of the VOU and generates a correctly sequenced

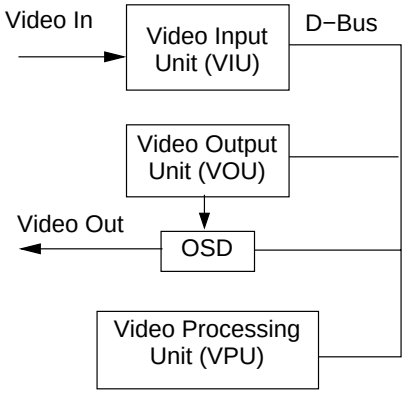

Fig. 3. Block diagram of Video Interface Unit.

ITU-R BT.601 or 656 4:2:2 output video stream. The VPU is a separate processing unit that operates in parallel with the VIU and VOU. A short description of its features is given later in this section. The flexible architecture of the VIO unit allows it to operate in a number of different configurations.

4.1. Video Encoding

Fig. 4 shows the flow of operations when the VIO is used in normal and intermediate encoding modes. In these modes, input video is captured by the VIU and is transferred to SDRAM. The buffered input is passed first to the VOU and then to the OSD unit, where it is mixed with text or graphics from the OSD buffers. The output of the OSD unit provides digital loop-back of the input video, overlaid with on-screen text or graphics.

If necessary, these modes also allow for additional preprocessing of the input video by the video processing unit (VPU). Among its functions, the VPU can initialize the video frame buffer with specific YCbCr values (e.g., blue screen generation), copy data from one video buffer to another, or scale data from one frame-buffer region to another frame-buffer region.

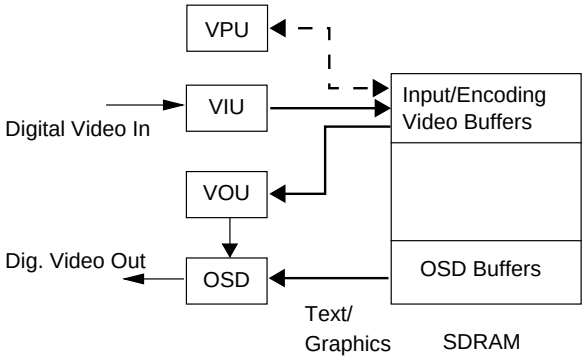

Fig. 4. VIO - Encoding, Normal and Intermediate modes.

When the VIO is configured in the advanced mode, input video can be mixed directly with OSD data and then passed back to the VIU and then to SDRAM for video encoding. Applications of this mode include the initial encoding screen menu set up, and real-time video scaling and editing at encoding. Using this advanced mode, users can also blend text and graphics into the input video that is being encoded.

4.2. Video Decoding Mode

Fig. 5 shows the flow of data in the VIO during video decoding. At minimum processing, decoded video data are

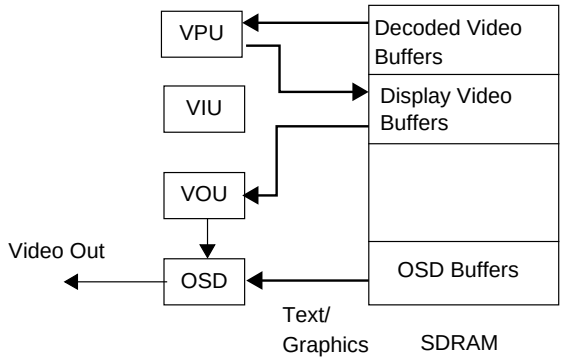

Fig. 5. VIO - Decoding mode.

transferred from the SDRAM to the VOU for chroma upconversion and other postprocessing. The output of the VOU is passed to the OSD where it can be mixed with text or graphics before it is transferred to the video output. Optionally, the VPU may also be enabled to process the decoded data before they are being transferred to the VOU. For example, the VPU can be used to scale-down specific video frames to create a thumbnail screen. Table 1 summarizes the key features of the codec.

5. IMPLEMENTATION AND STATUS

The codec is implemented using a standard-cell library in 0.18 μm CMOS technology. It uses an 108 MHz system clock.

6. CONCLUSIONS

In this paper we presented the architecture of single-chip MPEG-2, MP@ML, audio/video codec. By taking into consideration the overall system requirements in consumer-based digital video recording, we designed the codec with a unique and flexible video interface unit. The VIO can accommodate a variety of video pre- and postprocessing algorithms,

Video coding	MPEG-1, MPEG-2 MP@ML, SP@ML, I/P/B frames
Audio coding	Dolby Digital, MPEG (all layers)
Resolutions	up to 24-bit/sample
Resolutions	D1, 2/3 D1, 1/2 D1 CIF, SIF, QCIF
Rates	24, 25 , 29.97, 30 Hz
Prediction	Adaptive field/frame/16×8 Adaptive frame/field DCT Adaptive inter/intra
Rate Control	CBR, VBR (one-pass) I-only to 30 Mb/s
Interfaces	Video: ITU-601/656 I^2C,I^2S,SDRAM,EPROM, Flash,16-b/8-b parallel
Other	pre-, post-filtering 4:2:2 to 4:2:0 4:2:0 to 4:2:2 temporal/spatial filtering telecine, inverse telecine 8-bit OSD

Table 1. Key features of the Audio/Video Codec

thumbnail processing/editing, and loopback, in a very efficient way. Used with a standard DVD decoder, the codec can provide full-duplex DVD playback and recording functionality for time-shift or DVD-recordable applications.

7. ACKNOWLEDGMENTS

We would like to thank all the hardware and firmware engineers that have contributed to the design and implementation of this codec.

8. REFERENCES

[1] ISO/IEC JTC1 CD 13818. Generic coding of moving pictures and associated audio. International Organization for Standardization (ISO), 1994.

[2] C.T. Chen et al. A single-chip MPEG-2 video encoder/decoder for consumer applications. In *Proc. ICIP-99*. IEEE, 1999.

[3] C-Cube Microsystems. Dvxpress-mx25 and dvxpress-mx50. Product Brief, www.c-cube.com, 1999.

[4] Argonaut Technologies, Ltd. *ARC Interface Manual*, 1999.