DESIGN AND IMPLEMENTATION OF A MIXED-SIGNAL EMBEDDED DSP SYSTEM

Mark Yeary

Department of Electrical Engineering
Texas A&M University
College Station, TX 77843-3128

David Guidry, Mark Burns

Texas Instruments, Inc.
8505 Forest Lane, MS 8729
Dallas, TX 75266-0199

ABSTRACT

At Texas Instruments, integrated circuits in production are continually becoming more power efficient and faster. The time associated with testing these designs, say with a with Taradyne test platform, represents a large cost of the overall price of these integrated circuits. This paper discusses the design and layout of a compact mixed signal printed circuit board using a digital signal processor (DSP) that can be used in the test environment. In general, we live in an analog world, but the processing and transfer of information is typically digital. Mixed signal designs offer the best of both worlds since these designs can take advantage of the processing power of a DSP, while operating in close proximity to the analog signals. The paper presents a discussion of our design along with a picture of our mixed signal board, more detailed discussions and pictures may be viewed at http://ee.tamu.edu/∼mbyeary/mixedsignal.html

1. INTRODUCTION

DSP systems are gaining more prominence to solve a wide range of engineering problems as their processing power and functionality continue to increase. As it turns out, integrated circuits in production at Texas Instruments are continually exceeding the 1GHz clock rate. These high speed ICs produce major problems for the test engineer responsible for characterizing this product. The solution has typically been a trade off of bit resolution for speed. To solve this problem of bit resolution for speed, undersampling is typically employed. This particular design employs a swept delay generator that will sample a periodic waveform as depicted in Figure 1. The problem with this design is that the delay time, Δ, does not always factor evenly into the period, T, of the sampling waveform, i.e. $T \neq m\Delta$, given m an integer. This discontinuity introduces non-coherence into the sampled waveform. In other words, the swept delay generator does not have the ability to accurately modulate Δ, which is needed to provide coherent sampling. Moreover,

This work was supported by Texas Instruments, Dallas, TX.

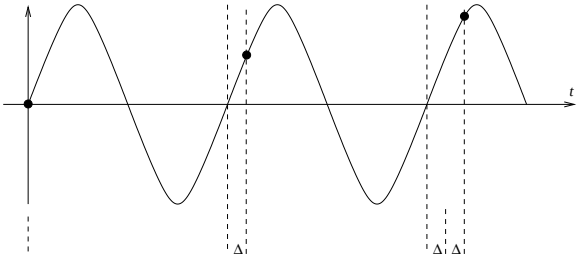

Fig. 1. Swept Delay Undersampling

Δ, is not always constant since the device that produces the delay is an analog device. Coherence is of prime importance, as reported in the current liturature [1][2]. Coherence implies that the test waveform is sampled over an integer number of cycles [3].

Coherence in a sampled waveform is preferred in order to use the Discrete Fast Fourier Transform (DFFT) which is commonly used to take measurements of gain, distortion, and signal to noise ratio. One technique to remedy the coherence problem is to window the data prior to processing [4]; however, windowing will cause a loss in the resolution [5]. Windowing also requires extra processing time, which is critical [3]. Other researchers have worked to sample over an integer number of cycles [3]. While this technique has proven effective, it assumes that the signal under test is slow enough for the A/D conversion strategy to provide an $n-$bit word at every sample point. As described below, we have employed a modified SAR technique [6] to digitize extremely high speed signals by assuming that it successively modifies only one bit of the $n-$bit word at every sample point over several cycles.

This paper provides a discussion of our mixed-signal DSP system, in the context of providing a solution to the coherence problem in high speed undersampling A/D conversion. Our device, the Coherent Undersampling Digitizer, is a DSP based circuit employs a new technique [6] that provides a method of maintaining clock speed and bit resolution without discontinuities in the output.

This paper is organized as follows. Section 2 provides the theoretical formulation of the sampling technique, while Section 3 discusses its implementation. Finally, Section 4 presents one example of our laboratory measurements.

2. THEORY OF OPERATION

The Coherent Undersampling Digitizer overcomes the problem of non-coherence by replacing the swept delay generator with a precise frequency ratio that generates evenly spaced sampling times. In this manner, the sampled waveforms are guaranteed to wrap around smoothly from the last sample to the first enabling the use of DFFTs for testing and calculations. The precise frequency ratio is achieved through the use of two clock generators with one set at a slightly lower frequency then the second. The comparator strobe is generated at a particular frequency, F_{sar}, which is slightly less that the frequency of the test signal, F_{utp}.

Referring back to Figure 1, it is possible to create the same undersampled set of samples, without the use of the swept delay generator. The difference being, we use a clocking signal which is running at a lower frequency that the signal under test, and it is not synchronized to it.

It is impossible to hold the delay time at a constant point for all samples to be taken for that point. For this reason, all the MSB comparisons must be performed first, then all the next lowest bits, and finally all the LSB comparisons are performed. The final digitized waveform must then be output by unshuffling these bits and sending them out in the proper order. The block diagram in Figure 2 depicts the arrangement of the hardware, as it resides on the printed circuit board.

As seen in Figure 2, the Coherent Undersampling Digitizer is a five chip solution. Only the comparator, DSP, and the DAC are the vital components of the design. The two translators (ECL-TTL and TTL-ECL) are incorporated into the design for voltage translation only. The logic levels between the comparator and DSP are unlike and therefore translation between the signals of each must take place.

As depicted in Figure 2, two frequencies are of prime importance. F_{sar} is the rate at which the comparator strobes, and F_{utp} is the frequency of the signal to be sampled. The theory behind the Coherent Undersampling Digitizer is that the frequency source controls these two frequencies must be set using a precise ratio to produce a linear controlled slip in comparator strobe times. This ratio is

$$F_{sar} = \left[\frac{S}{S+1}\right] F_{utp} \ . \qquad (1)$$

The frequency source that governs F_{sar} is precisely set at a lower frequency than the frequency source that governs F_{utp}. The variable S represents the number of samples to be taken in one period the signal to be sampled. To facilitate subsequent DFFT analysis, S should be a power of 2, i.e, $S = 2^m$, given m is an integer.

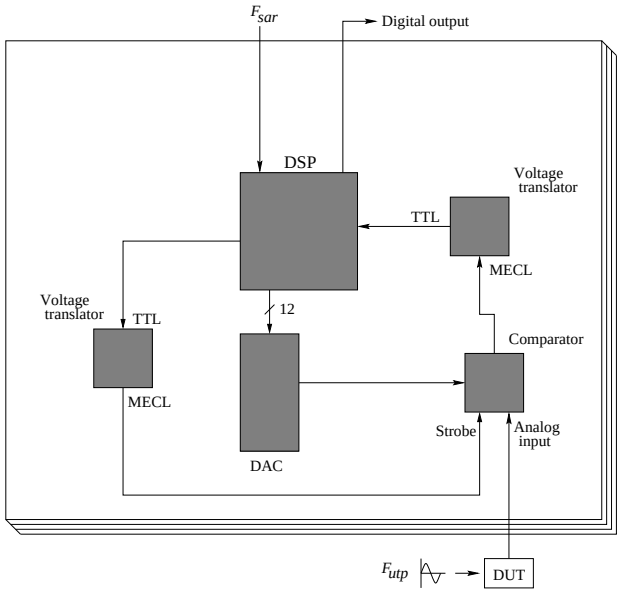

Fig. 2. Block diagram depicting components and functions on the multi-layer printed circuit board. The DSP is used to store the digitized samples of the Device Under Test (DUT) and to control the DAC and comparator.

3. IMPLEMENTATION DETAILS

Using a digital signal processor (DSP) proved to be ideal since a bank of waveform capture random access memory (RAM) is necessary to temporarily store the resulting digitized samples. The Texas Instruments TMS320F206 DSP was chosen. The 'F206 is a 16-bit fixed point DSP capable of operating at speeds up to 20 million instructions per second. The DSP's software was written with Code Composer, a development system by Go DSP. As it turns out, much of the functionality cost can be embedded into the software of a DSP, as opposed to extra hardware [7].

As depicted in Figure 2, the analog output of the DAC is the signal compared to the input signals of the DUT. This comparison allows the SAR algorithm a basis to make its bit decision. The selection of the DAC was based on its resolution and settling time. With 12-bits parallel input, the TLV5619 provided enough resolution for the signals being digitized. Since the algorithm is based on a precise frequency ratio, the ideal case is to have the entire algorithm and DAC output available instantaneously. Since this is unrealistic, the lower the settling time of the DAC the better. The execution speed of the 'F206 DSP is not an issue. With a nominal $1ms$ ($3ms$, worst case) settling time the DSP

code must provide a delay between writes to the DAC.

As part of the SAR, an MC10E1651 comparator was used. The selection of this chip was based on its high speed. The comparator receives an input signal from the DUT (device under test). This voltage is compared to the output signal of the DAC, which initially is set to mid scale in reference to the reference input of the DAC. This comparison output is sent through the MECL/TTL translator to the DSP as part of the SAR routine. The latch signal is received from the DSP, through the TTL/MECL translator to the comparator. When the latch enable is at a logic level high the MC10E1651 acts as a comparator and when the latch enable input goes to a low logic level, the outputs are latched. The comparator is ECL logic and therefore the outputs will be pure differential ECL levels.

The comparator strobe rate was very important, so it was examined during the first part of the design. While digitizing a signal, the DSP is running a looping program. In this loop there are 4 different paths that can be taken, depending on the SAR routine. No matter which route was taken the same amount of time needed to have passed between comparator strobes, otherwise F_{sar} would not be constant. The number of clock cycles that have passed determines the time between comparator strobes. Each instruction of the DSP assembly code has a slightly different number of clock cycles. The number of clock cycles was determined by allowing the comparator to properly settle between strobes. Therefore equation (1) was modified to become

$$F_{sar} = \left[\frac{S \cdot N}{S \cdot N + 1} \right] F_{utp} \ . \qquad (2)$$

The integer N denotes the number of clock cycles that must pass between each compare strobe. Since we ran our DSP at approximately 20 MHz, selecting $N = 167$ proved to be sufficient while taking laboratory measurements.

Figure 3 depicts a picture of our new device. The Coherent Undersampling Digitizer board was designed to be compact in size, about the size of a business card. Its final dimensions were 2700 mils $\times$ 2200 mils (68.58mm $\times$ 55.88mm). The thickness of this four layer board was 62.5 mils (1.59mm). The board was designed using four layers. The primary reason for this was to isolate the ground and power from the sensitive signals of the CUD. The layers were established as follows. Layer 1: signal, layer 2: ground plane, layer 3: split power plane, layer 4: signal. To reduce the effect of noise on the signals, decoupling capacitors were used on all power pins. Since the comparator and the translators require both ± 5 V, the board included a split power plane. By careful placement of all of the devices, the split plane satisfied their voltage requirements, without introducing the extra cost of an additional plane.

Since the digitized output of the DAC has the possibility of exceeding 1 GHz, shielding the signal from noise was extremely important. On the board layout, this was accomplished by providing a guard trace [8] around the analog output at all connections. This trace was then connected to ground through a via. By shielding the signal with a grounded trace, the analog output becomes less susceptible to noise interference from other signals. In general, the frequency content of each signal was examined. High speed lines were laid out on 45° angles to prevent reflections [9].

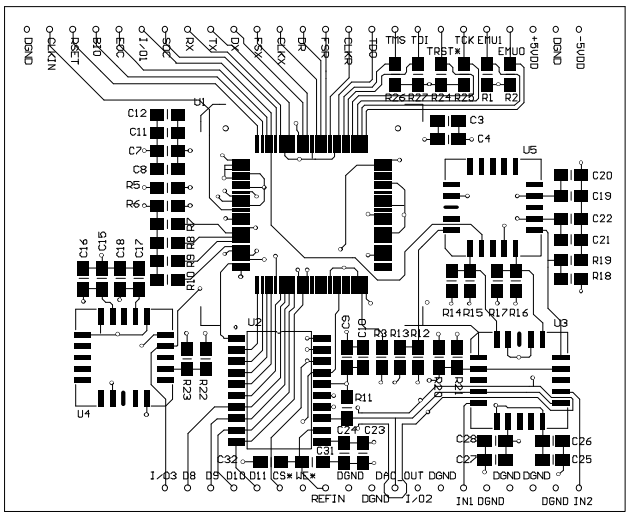

Fig. 3. Top Layer of the Multi-Layer Mixed-Signal Embedded DSP System

4. LABORATORY MEASUREMENTS

As a representative example of our laboratory experiments, we examined the rise time of a periodic square wave, as depicted in Figure 4. The signal was quantized with 12 bits of resolution. The number of samples was assigned to be $S = 128$ and the following settings were made: $F_{utp} = 20,000,235$ Hz, $F_{sar} = 19,999,299$ Hz. It took 5 digital samples to span 10 - 90% full scale, which relates to a 1.9531 ns rise time. While this degree of resolution may seem very high, it is on a par with the high rates achieved with beat frequency testing [10]. The difference however, is that our sample set is coherent.

We would like to mention that coherent sampling of signals is not new. To point out a philosophical difference, Tangelder [11] discusses coherent sampling, but he assumed that the signal under test is slow enough for the A/D conversion strategy to work at every sample point. In our paper, we developed a modified SAR technique to digitize higher speed signals. The basic principle is that it successively modifies only one bit of the $n-$bit word at every sample point over several cycles and holds the bits of all of the samples in the memory of a DSP chip, without the use of a swept delay generator. It should also be mentioned that

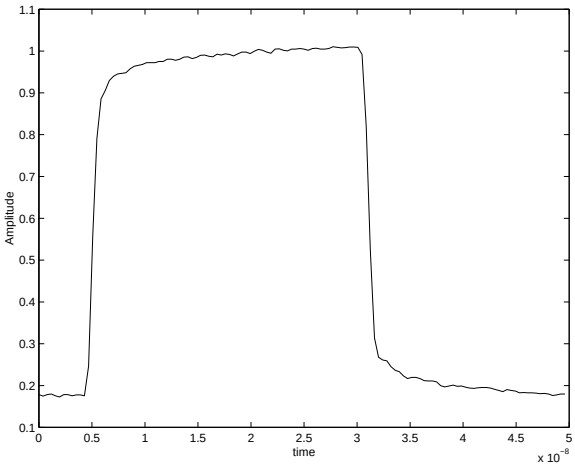

Fig. 4. Laboratory Data Depicting a Coherently Digitized Square wave

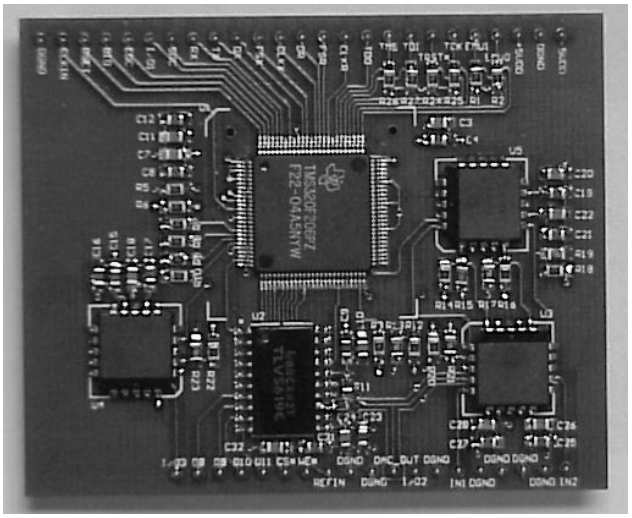

Fig. 5. Mixed-Signal Embedded DSP System

a 20 MHz signal can easily be digitized using traditional converters. By incorporating a faster comparator, say one rated at 1GHz, we expect to digitize much higher frequency signals. The examples do not push our digitizer into the frequency range where its advantage is eminent.

5. SUMMARY

Figure 5 depicts our DSP system. By applying analog and digital design techniques, we have been able to take advantage of a DSP's processing power and internal memory to digitize high speed signals and produce coherent sequences of samples with relatively high resolution without the traditional employment of a swept delay generator. The desire for a coherent digitized output comes from the need of test algorithms such as DFFTs. These algorithms require coherency in the signal in order to work. Later additions to this project will involve writing code on a Teradyne which will automatically program the 'F206. This is possible through the on-chip synchronous serial port of the 'F206.

6. REFERENCES

[1] P. Carbone and G. Chiorboli, "ADC sinewave histogram testing with quasi-coherent sampling," *Proc. IMTC*, vol. 1, pp. 108-113, 2000.

[2] M. Burns and G. Roberts, *An Introduction to Mixed-Signal Testing*. New York: Oxford Univ. Press, 2000.

[3] J. Mielke, "Frequency domain testing of ADC's," *IEEE Design & Test of Computers*, vol. 13, No. 1, pp. 64-69, 1996.

[4] M. Demler, *High-Speed Analog-to-Digital Conversion*. San Diego, California: Academic Press, 1991.

[5] F. Harris, "On the use of windows for harmonic analysis with the discrete Fourier transform," *Proceedings of the IEEE*, vol. 66, No. 1, pp. 51-83, 1978.

[6] M. Burns, *Coherent undersampling digitizer for use with automatic field test equipment*. U.S. Patent, US5589763, 1995.

[7] G. Goossens, *et. al.*, "Embedded software in real-time signal processing systems: design technologies," *Proc. of the IEEE*, vol. 85, issue 3, pp. 436-454, 1997.

[8] H. Johnson and M. Graham, *High-Speed Digital Design*. New Jersey: Prentice Hall PTR, 1993.

[9] G. Ginsberg, *Printed Circuits Design*. New York: McGraw-Hill, 1991.

[10] C. Coombs, *Electronic Instrument Handbook*. New York: McGraw-Hill, 1995.

[11] R. Tangelder, H. de Vries; R. Rosing, H. Kerkhoff, M. Sachdev, "Jitter and decision-level noise separation in A/D converters," *Proc. IMTC*, vol. 3, pp. 1558-1562, 1999.