FPGA IMPLEMENTATION OF A TUNABLE BAND-PASS FILTER USING THE "BASIC HETERODYNE BLOCK"

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ABSTRACT

Any Band-Pass filter may be converted into a tunable filter with a single tuning parameter through the use of a new Tunable Heterodyne Band-Pass Filter concept in which the frequency of the heterodyne signal is adjusted thereby translating the entire filter transfer function in frequency. If the fixed filter is selected to be a narrow-band band-pass filter, the new Tunable Heterodyne Band-Pass Filter concept can be used very effectively in the elimination of narrow band interference in wide-band communications or control systems. A single-chip version of this tunable filter can be constructed using a Xilinx Virtex XCV800 chip. The resulting filter is a flexible tunable band-pass filter that can be varied from DC to $\pi/2$ or from $\pi/2$ to π depending on the parameters of the fixed output low-pass filter.

1. INTRODUCTION

Modern wireless and satellite communications systems make use of Frequency-Hoping Spread-Spectrum (FHSS) and Direct-Sequence Spread-Spectrum (DSSS) modulation systems which spread the energy of the communications signal across a wide band of frequencies allowing for simultaneous use of the channel by multiple users [1], [2], [3], [4]. However, strong narrow-band signals from standard AM and FM radio transmissions within the communications channel can saturate these modulators thus making it impossible to detect the spread-spectrum signal [5], [6], [7], [8]. Similarly, in many control applications a narrow-band mechanical resonance can interfere with the feedback control signals from various transducers making it impossible to detect and control the parameters of the plant [9], [10]. In many of these situations it is not possible to use a fixed filter to eliminate the narrow-band interference because either there are many interfering signals popping on and off at different times and frequencies or the frequency of the narrow-band interfering signals is time-varying such as the case of a mechanical resonance varying in frequency as temperature changes [9]. In these situations, a tunable narrow-band filter for attenuation of the narrow-band interference is required.

2. TUNABLE HETERODYNE BAND-PASS FILTER

2.1 Basic Concept

In an earlier paper [11] we introduced the basic tunable heterodyne filter block and showed how this could be used as an adaptive filter in either a communications systems application or a control systems application. The basic concept of the Tunable Heterodyne Band-Pass Filter is quite similar to the concept of super-heterodyne used for radio signals. As in a super-heterodyne radio receiver, Intermediate Frequency (IF) signal is mixed (heterodyned) with the incoming signal to translate the detection and demodulation problem to a fixed-frequency spectrum in which it is most convenient to implement the detector and demodulator. Similarly, the Tunable Heterodyne Band-Pass Filter system mixes an IF signal with the input signal to translate the filtering problem to a fixed frequency where it is convenient to do the filtering operation [10]. In this paper we develop a detailed Xilinx FPGA implementation of this filter and provide experimental measurements to show a close match with simulation results from Matlab.

2.2 Basic Heterodyne Block

Figure 1 shows the block diagram for the Tunable Heterodyne Band-Pass Filter, which consists of three key elements. A brief explanation of these elements is given below:

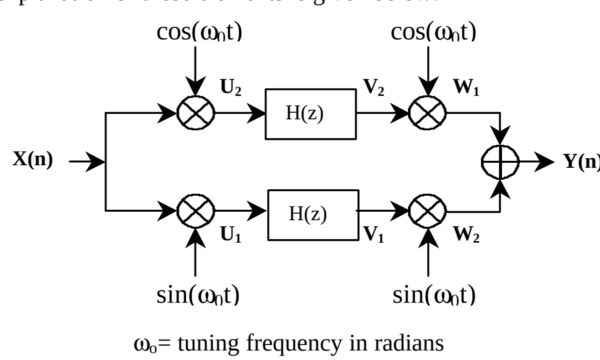

Figure 1. *Heterodyne Band-Pass Filter block diagram.*

i. **Splitter:** A direct digital up-converter that multiplies the input signal by sine and cosine of the heterodyne frequency to create the intermediate frequency quadrature signals.

ii. **Prototype Filter:** The fixed digital filter (band-pass in this case) that generates the tunable filter over a certain range of frequencies. This filter may be IIR and may be of high order without affecting the complexity of the tuning algorithm.

iii. **Combiner:** A direct digital down-converter that multiplies the intermediate frequency quadrature signals (one signal by sine and a second signal by cosine) and then sums ($W_1 + W_2$ in Figure 1) the two signals to create the base-band signal.

2.3 Splitter

The first part of our Tunable Heterodyne Band-Pass filter is a structure called the "Splitter". An 8-bit signed input signal is fed into this circuit, which is multiplied (Heterodyned) with sine and cosine to produce two separate outputs (U_1 and U_2 in Figure 1). The sine and cosine frequency is the tuning frequency that translates the incoming signal to the fixed band-pass frequency. As described in the previous paper [13], two look-up tables were created from Xilinx Core Generator to implement the sine and cosine functions. This can later be replaced with a look-up table constructed from either VHDL or Verilog. The rate at which we step through the sine and cosine coefficients determine the tuning frequency for the application. The Core Generator was also used to implement the 8-bit multipliers used for heterodyning purposes. The total number of CLB count for the Splitter circuit is 128.

2.3.1 Splitter Simulation

A simulation of the splitter was produced with Matlab and the results were confirmed with actual experimental data. With a sampling frequency of 48 kHz, the heterodyne frequency (in this case) was set to 2500Hz and input signal frequency was set to 15,200Hz. Figures 2 and 3 show the Matlab simulation and the actual experimental plot respectively. Figure 4 shows the two superimposed on one graph.

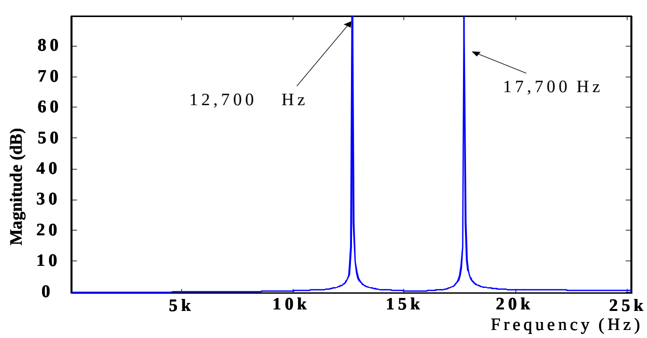

Figure 2. *FFT response of "Splitter" simulation results*

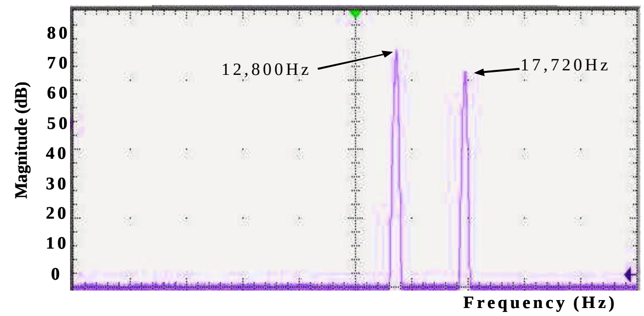

Figure 3. *FFT response of* ***"Splitter" experimental results.***

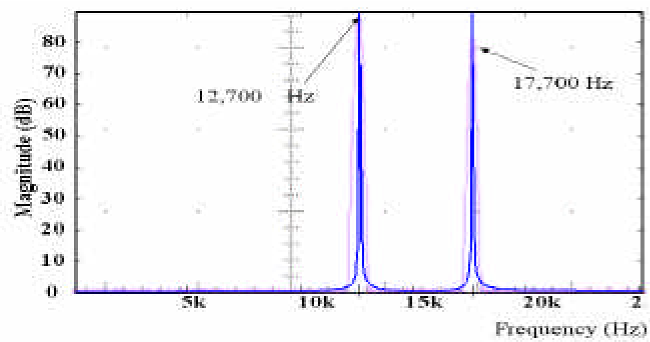

Figure 4. *Superimposed simulation and experimental results.*

2.4 Prototype Filter (Band-Pass)

For implementation of our Tunable Heterodyne Band-Pass Filter, we chose a narrowband second order IIR Band-Pass Filter to be used as our fixed filter structure. In order to achieve the desired effect of a tunable band-pass structure, both the filters used in Figure 1 must have identical transfer functions. Our band-pass filter is designed to have maximum gain at quarter of the sampling frequency and is developed using the following equation:

$$H(z) = \frac{(1-a)(1-z^{-2})}{2(1+a\ z^{-2})}, \qquad where\ a = 7/8 = 0.875\ldots\ldots(1)$$

The Splitter circuit translates the input signal to the fixed frequency of the band-pass filter, which allows the band-pass filter to select out the interference from the input signal. This interference signal can later be used in an adaptive structure where it will be removed.

2.4.1 Band-Pass Filter Simulation

Figure 5 shows the actual experimental results superimposed onto the Matlab simulation results. The center frequency of the band-pass filter will be at $f_s/4$ where f_s is the sampling rate, which is 48kHz for our example. The peak is right at the predicted value of 12kHz and matches the Matlab data very well down to about 20db. Below 20db, the experimental results vary slightly from predicted, but it was also very hard to take data in

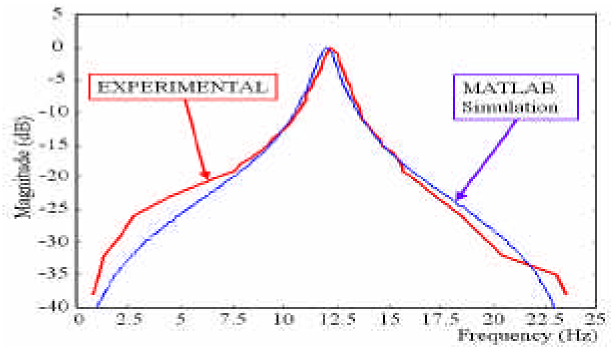

Figure 5. *Band-pass magnitude response comparison plots*

this region, so there may be some experimental error. The total number of CLBs for the band-pass filter is 54.

2.5 Combiner

The final part of our Tunable Heterodyne Band-Pass filter (Figure 1) is the "Combiner" structure. The 8-bit outputs of both the band-pass filter is fed into each branch of this circuit, (Figure 1) which is again Heterodyned to produce two separate outputs and then summed using an adder to bring the signal back to its base band. The total number of CLB count for the Combiner circuit is 130.

2.5.1 Combiner Simulation

Figures 6 and 7 show Matlab simulation results and experimental results respectively. In this case, the Combiner was tested with an input signal at 5000Hz, which is then heterodyned with the tuning signal at 1000Hz to produce peaks at 4000Hz and 6000Hz respectively. The maximum gain of the filter is at 12kHz, which is $f_s/4$. As shown, the data closely matches Matlab's results for the given experiment. Figure 8 shows the superimposed image from the data of Figures 6 and 7.

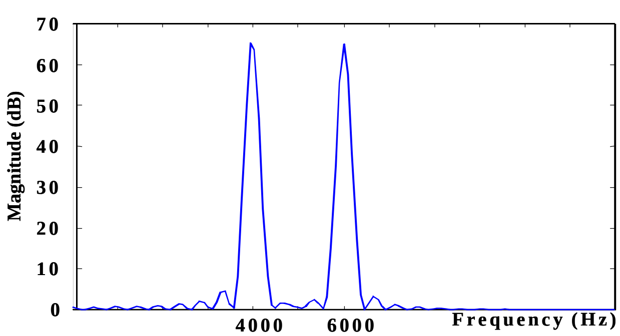

Figure 6. *FFT response of* ***"Combiner" simulation results.***

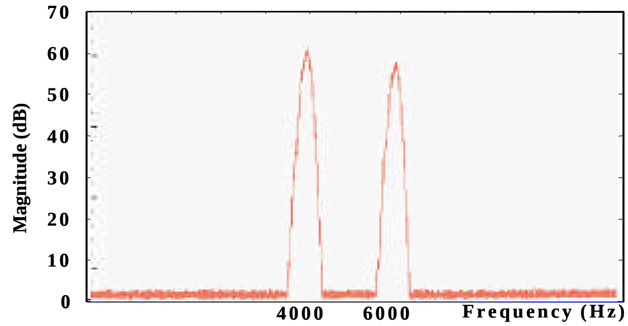

Figure 7. *FFT response of* ***"Combiner" experimental results.***

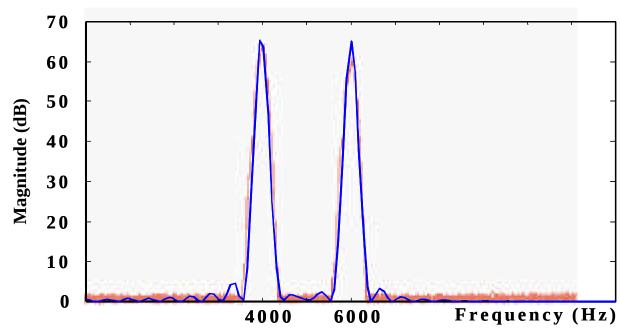

Figure 8. Superimposed Combiner simulation and experimental results.

5. FINAL RESULTS

Figure 9 shows the final results of the hardware implementation of the Tunable Band-pass Filter against the Matlab simulation results obtained using an input error signal of 10kHz and a tuning frequency of 2kHz.

6. COMPARISON

In this section, we present a comparison between our method of implementing an N^{th}-order tunable band-pass IIR filter and the conventional method of implementation without the heterodyne process. An estimation of the hardware and complexity reduction between a conventional method that may be used to

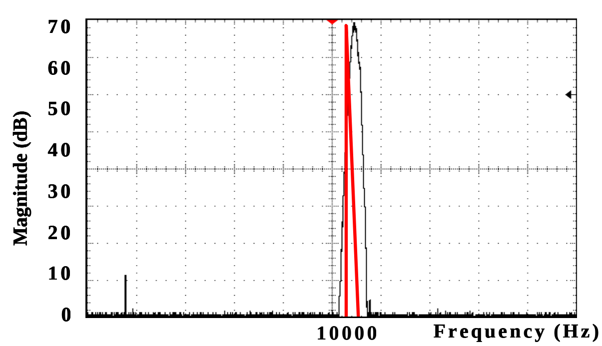

Figure 9. Superimposed final simulation and experimental results.

implement a tunable filter and the method proposed in this paper can be shown in Table I. We are assuming an N^{th}-order Direct Form II realization of the band-pass filter in each case. In the case of the standard technique, we assume that each of the filter coefficients is derived from a ROM that stores (N+1) 8-bit coefficients for each of the M discrete frequencies that the filter can be tuned to. The heterodyne filter has the advantage that it can be tuned continuously, while the standard filter can only be tuned to the M pre-chosen frequencies whose filter coefficients are stored in the ROM. The last line in the table gives the total CLB's for each of the filters in terms of N and M. To find the value of M for which the two filters will have an equal number of CLB's, we set the two totals equal and solve for M:

$$M = \frac{8(169 - 6N)}{18N - 9} \qquad (2)$$

For our 2^{nd}-order band-pass filter the 3db bandwidth is 500Hz. If we were to design the standard Direct Form II second-order filter such that it could be tuned anywhere between DC and the Nyquist frequency (24kHz) in increments of 500Hz, this would require M=48. However, for N=2 in equation (2) we obtain a value of M=46.5 indicating that the heterodyne technique would use less hardware for any value of M greater than 46.5. Thus for M=48, even our second-order heterodyne filter is superior to the standard filter. For higher-order filters the break-even point is even less, so the heterodyne approach appears to offer an excellent solution to the problem of tunable IIR filters.

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Table I. Comparison of Heterodyne Tunable Filter to Standard Tunable Filter

Component	CLB's Per component	Heterodyne Filter	CLB's in Heterodyne Filter	Standard Filter	CLB's in Standard Filter
Adders	8	4N+1	32N+8	2N	16N
Delays	4	2N	8N	N	4N
Fixed-Coefficient Multipliers	4	4N-4	16N-16	0	0
Variable-Coefficient Multipliers	21	4	84	2N-1	42N-21
64-Bit ROM's	9	8	72	(2N-1)M/8	9(2N-1)M/8
TOTAL			56N+148	62N+9(2N-1)M/8-21	

Note: N is the order of the IIR filter and M is the number of frequencies that the standard filter can be tuned to. The heterodyne filter is continuously tunable while the standard filter can only be tuned to M distinct frequencies.