THE MISMATCH-NOISE PSD FROM A TREE-STRUCTURED DAC IN A SECOND-ORDER $\Delta\Sigma$ MODULATOR WITH A MIDSCALE INPUT

Jared Welz, Ian Galton
University of California, San Diego, 9500 Gilman Drive, La Jolla, CA 92093-0407, USA

ABSTRACT

Mismatch-shaping DACs have become widely used in high-performance delta-sigma data converters in recent years. Nevertheless, no theoretical results have been published to date that quantify their performance, so designers have been forced to rely on simulation-based analyses. This paper presents the first theoretical performance analysis of a mismatch-shaping DAC. Specifically, the PSD of the mismatch noise introduced by a first-order tree-structured DAC within a second-order ADC delta-sigma modulator with a midscale constant input signal is derived. This particular mismatch-shaping DAC and delta-sigma modulator configuration was chosen for analysis because it has been demonstrated experimentally to achieve state-of-the-art ADC performance. The choice of a constant midscale input was made because simulation and experimental results suggest that it yields the worst-case performance.

1. INTRODUCTION

Delta-sigma ($\Delta\Sigma$) modulators used for analog-to-digital (A/D) conversion tend to be highly sensitive to signal-band noise introduced by the DACs in their feedback paths. In switched-capacitor DACs, which are the type most commonly used in $\Delta\Sigma$ modulators, the dominant noise component is *mismatch noise* which arises from static DAC output level errors caused by fabricated component mismatches. Therefore, mismatch-shaping DACs, which use spectral shaping to minimize the signal-band power of the mismatch noise, have become widely used in state-of-the-art $\Delta\Sigma$ modulator based ADCs [1]-[3]. However, the mismatch-shaping performance of these DACs has been demonstrated only with simulations and experimental measurements; to the knowledge of the authors, no theoretical results have been published previously that quantify their mismatch-shaping performance. The dearth of such results has forced designers to rely on computer simulations to estimate the worst-case performance of candidate architectures during the design process.

This paper presents the first theoretical performance analysis of a mismatch-shaping DAC. The analysis applies to a tree-structured DAC within the second-order $\Delta\Sigma$ modulator shown in Fig. 1, which is a system that has been shown to yield state-of-the-art experimental results [3]. In both tests and simulations of the system, it was observed that the DAC generated the worst-case signal-band mismatch noise when the input was a midscale dc signal. This paper analyzes the performance of the tree-structured DAC in this setting as a potential bound to its performance. The analysis provides theoretical power spectral density (PSD) curves for the DAC mismatch noise.

2. THE TREE-STRUCTURED DAC

A 9-level example of the tree-structured DAC is shown

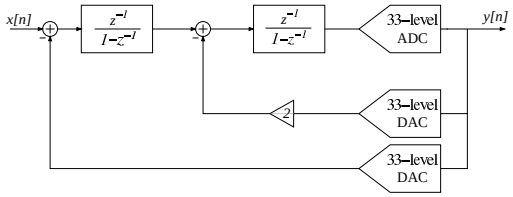


Fig. 1: The second-order, analog $\Delta\Sigma$ modulator.

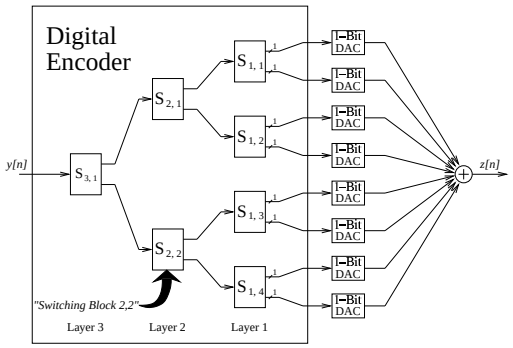


Fig. 2: An example 9-level tree-structured DAC.

in Fig. 2. It consists of a *digital encoder* and a bank of 1-bit DACs. The digital encoder selects exactly $y[n]$ of the 1-bit DACs to have high inputs and the remaining $8 - y[n]$ of the 1-bit DACs to have low inputs. For most values of $y[n]$, this can be done in many ways, and this flexibility is exploited by the digital encoder to realize the desired spectral shaping of the mismatch noise. The 1-bit DACs are called *DAC elements*. The analog output of the *i-th* DAC element is given by

$$z_i[n] = \begin{cases} 0.5 + e_{h_i}, & y_i[n] = 1; \\ -0.5 + e_{l_i}, & y_i[n] = 0; \end{cases} \tag{1}$$

where $y_i[n]$ is the input bit, and e_{h_i} and e_{l_i} are the high and low errors of the *i-th* DAC element, respectively.

The selection of DAC elements is determined by the operation of the *switching blocks* that constitute the digital encoder. Each switching block is labeled $S_{k,r}$ in the figure, where k is its horizontal layer number and r is its vertical depth within the layer. The $S_{k,r}$ switching block outputs are

$$x_{k-1,2r-1}[n] = \tfrac{1}{2}(x_{k,r}[n] + s_{k,r}[n]), \tag{2}$$

and

$$x_{k-1,2r}[n] = \tfrac{1}{2}(x_{k,r}[n] - s_{k,r}[n]), \tag{3}$$

where $x_{k,r}[n]$ is the switching block input, and $s_{k,r}[n]$ is a *switching sequence* generated within the switching block. The switching sequence $s_{k,r}[n]$ is ± 1 when $x_{k,r}[n]$ is odd, and 0 otherwise.

In [4], it is shown that the DAC mismatch noise is a linear combination of these switching sequences. Therefore, the mismatch noise is spectrally shaped if each switching block generates a shaped switching sequence. For the first-order DAC, the switching sequences are generated using symbols of the form

$$[1\,0\cdots0\,-1\,0\cdots0] \text{ and } [-1\,0\cdots0\,1\,0\cdots0], \quad (4)$$

where each zero corresponds to an even switching block input, so the zero runs vary in length. At the end of each symbol, the next symbol type is selected randomly from the two possible symbol-type choices. The random selection is made independently from the previous symbol choices with a probability of 0.5 for each symbol.

3. THE DAC-NOISE PSD

This section presents expressions for the theoretical mismatch-noise PSD of the DAC in the described system, and presents an example which demonstrates that the theoretical mismatch-noise PSD precisely matches the mismatch-noise PSD obtained using computer simulation. The expressions are the result of an analysis sketched in the following sections. They express the mismatch-noise PSD as a function of the DAC-element errors, which, as noted previously, are consequences of fabricated component mismatches and are taken to be constants. Regardless of how these errors are distributed, the mismatch-noise PSD from the DAC is spectrally shaped, and the expressions accurately describe the corresponding PSD.

Fig. 3 shows the simulated and theoretical versions of DAC mismatch-noise PSD for a representative example. In this example, as in all those observed by the authors, the theoretical PSD would lie almost entirely on the simulated PSD if the curves were plotted on the same axis. The DAC-element errors used in the example were chosen arbitrarily as a collection of independent and identically distributed (i.i.d.) Gaussian random variables with zero mean. The standard deviations of the DAC-element errors were chosen to be 0.3% of the DAC's nominal step size which corresponds to reasonable matching precision by the standards of present-day switched-capacitor CMOS circuit technology. The resulting DAC-element errors were used to calculate the theoretical mismatch-noise PSD and to obtain the simulated mismatch-noise PSD. The remaining components in the simulated $\Delta\Sigma$ modulator were modeled as ideal circuits. The input to the $\Delta\Sigma$ modulator was a sequence of i.i.d. Gaussian random variables with zero mean and standard deviations of 0.1% of the ADC step size, Δ. This random process accurately models the kT/C noise associated with the first-stage sampling capacitors in the $\Delta\Sigma$ modulator in [3].

The theoretical DAC-noise PSD is given by

$$S_{ee}\left(e^{j\omega}\right) = \sum_{k=1}^{b} \Delta_k S_k\left(e^{j\omega}\right),$$

where b is the number of layers in the DAC (*i.e.,* 5 in this example); with $\delta_i = e_{h_i} - e_{l_i}$,

$$\Delta_k = \sum_{r=0}^{2^{b-k}-1} \left[\frac{1}{2^k} \sum_{i=r2^k+1}^{r2^k+2^{k-1}} \delta_i - \delta_{i+2^{k-1}} \right]^2; \quad (5)$$

and $S_k\left(e^{j\omega}\right)$ is constructed below for the cases of $k = 1$ and $k > 1$.

For $1 < k \leq b$,

$$S_k\left(e^{j\omega}\right) = 4\sum_{n=1}^{\infty} P_k(n,0)\sin^2\left(\frac{\omega n}{2}\right), \quad (6)$$

where $P_k(n,m)$ is evaluated using the recursive equation

$$P_{k-1}(n,m) = \sum_{i=m}^{\lfloor (n-1)/2 \rfloor} \left(\tfrac{1}{2}\right)^{i+3} \left(\tbinom{i}{m} + 2\tbinom{i-1}{m-1} \right) P_k(n,i), \quad (7)$$

with the convention $\binom{i-1}{-1} = \delta[i]$. The initial condition (at $k = b$) for (7) is

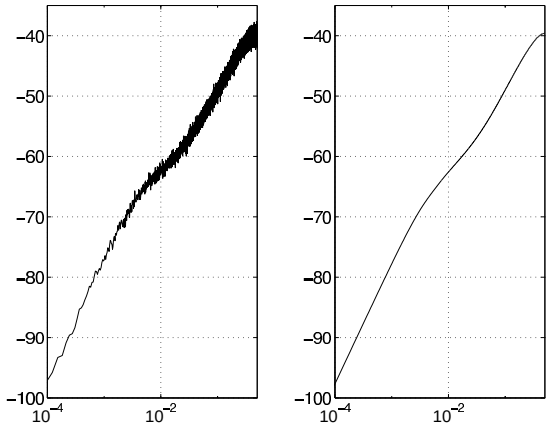
$$P_b(n,m) = \begin{cases} 0, & m > \frac{n-1}{2}; \\ \frac{(m+1)^2}{n(n+1)(n+2)} + \frac{m^2}{n(n-1)(n-2)}, & n > 2, m < \frac{n-1}{2}; \\ \frac{(m+1)^2}{n(n+1)(n+2)}, & \text{otherwise.} \end{cases} \quad (8)$$

For $k = 1$,

$$S_1\left(e^{j\omega}\right) = 2\left[1 - 4p_1 + 2p_2\right]\sin^2\left(\frac{\omega}{2}\right) + 4\sum_{n=2}^{\infty}\left[p_{n-1} - 2p_n\right]\sin^2\left(\frac{\omega n}{2}\right), \quad (9)$$

where

$$p_n = \begin{cases} \frac{\left[\left(\frac{1}{2}\right)^{b-1}\right]\frac{n+1}{2}}{4n}, & n \text{ odd}; \\ \left(\frac{3}{4}\right)^{b-1}\left(\frac{n\left[\left(\frac{1}{2}\right)^{b-1}\right]\frac{n}{2}}{4(n-1)(n+1)}\right), & n \text{ even}. \end{cases} \quad (10)$$



(a) (b)

Fig. 3: The DAC-noise PSD from a) simulation and b) theory.

4. THE SWITCHING-SEQUENCE PSD

As previously mentioned, the DAC mismatch noise is a linear combination of the switching sequences. The $S_k\left(e^{j\omega}\right)$ function in the previous section is the PSD of each switching sequence in layer k. The derivation of these PSDs is described following some additional definitions.

The symbols shown in (4) are partitioned into two "halves." The first half of the symbol—*i.e.*, the first $\pm 1\ 0\ \cdots\ 0$—is called the *head* of the symbol, and the second half is called the *tail*. Thus, each switching sequence value is an *element* of either the head or tail of some symbol. The only nonzero elements within a given symbol are the head's first element and the tail's first element.

Samples in different symbols are uncorrelated because the type of each symbol in the switching sequence is chosen randomly . However, the resulting switching-sequence PSD is still a function of the input's statistics because the magnitude of the switching sequence is a function of the switching block input. For now, consider the switching block input to be a deterministic sequence. Additionally, enumerate the symbols in increasing order with the first symbol beginning at sample $n = 0$. Because inter-symbol samples of $s_{k,r}[n]$ are uncorrelated, it is convenient to view $s_{k,r}[n]$ as a sum of windowed sequences:

$$s_{k,r}[n] = \sum_{i=1}^{\infty} s_{k,r}[n] w_i[n], \tag{11}$$

where $w_i[n]$ is 1 if $s_{k,r}[n]$ is an element of the *i-th* symbol and 0 otherwise. The random symbol-type choices cause the windowed sequences to be uncorrelated: for all n, m, and $i \neq j$,

$$E\left[s_{k,r}[n]\, w_i[n]\, s_{k,r}[m]\, w_j[m]\right] = 0; \tag{12}$$

where E is the ensemble-average expectation operator.

To exploit the orthogonality between these windowed sequences, the PSD of $s_{k,r}[n]$ is computed by obtaining its periodogram. Let N_s be the number of samples of $s_{k,r}[n]$ that compose its first N symbols, and let $P_N\left(e^{j\omega}\right)$ be the periodogram of $s_{k,r}[n]$ across these samples:

$$P_N\left(e^{j\omega}\right) = \frac{1}{N_s}\left|\sum_{n=0}^{N_s-1} s_{k,r}[n] e^{-j\omega n}\right|^2. \tag{13}$$

Substituting (11) into (13) gives

$$P_N\left(e^{j\omega}\right) = \frac{1}{N_s}\left|\sum_{n=0}^{N_s-1}\sum_{i=1}^{N} s_{k,r}[n]\, w_i[n] e^{-j\omega n}\right|^2. \tag{14}$$

For a given collection of N symbols, the types of these symbols can be assigned in several different ways, all of which are equally probable. By averaging over these symbol-type selections, the orthogonality given by (12) can be exploited to simplify (14). Let $S_N\left(e^{j\omega}\right)$ be the expected value—averaged over the random symbol-type choices—of the periodogram in (14): $S_N\left(e^{j\omega}\right) = E\left[P_N\left(e^{j\omega n}\right)\right]$. Upon rearranging the order of summation, this averaged periodogram is

$$S_N\left(e^{j\omega}\right) = \frac{1}{N_s} E\left|\sum_{i=1}^{N}\left(\sum_{n=0}^{N_s-1} s_{k,r}[n]\, w_i[n] e^{-j\omega n}\right)\right|^2. \tag{15}$$

From the orthogonality of the cross-products, as given by (12), and the linearity of the expectation operator, it follows that

$$S_N\left(e^{j\omega}\right) = \sum_{i=1}^{N} E\left[\frac{1}{N_s}\left|\sum_{n=0}^{N_s-1} s_{k,r}[n]\, w_i[n] e^{-j\omega n}\right|^2\right]. \tag{16}$$

Therefore, $S_N\left(e^{j\omega}\right)$ is the sum of averaged periodograms of the windowed sequences $s_{k,r}[n]w_i[n]$. In these sequences, there are exactly two nonzero samples, and these samples alternate in sign. The type of the *i-th* symbol determines the sign of the first nonzero sample in the sequence $s_{k,r}[n]w_i[n]$, but it has no affect on its periodogram. Thus, the periodogram of the sequence $s_{k,r}[n]w_i[n]$ is not a function of the symbol-type choices, and (16) can be simplified to

$$S_N\left(e^{j\omega}\right) = \sum_{i=1}^{N} \frac{1}{N_s}\left|\sum_{n=0}^{N_s-1} s_{k,r}[n]\, w_i[n] e^{-j\omega n}\right|^2. \tag{17}$$

The periodogram of each windowed sequence is a function of the number of zeros between its two nonzero samples. Specifically, it can be verified that

$$S_N\left(e^{j\omega}\right) = \sum_{i=1}^{N} \frac{4}{N_s} \sin^2\left(\frac{\omega H_i}{2}\right), \tag{18}$$

where H_i is the head length (*i.e.*, number of samples in the head) of the *i-th* symbol. To further simplify (18), note that the sample variance of $s_{k,r}[n]$ in this interval is

$$\bar{\sigma}_N^2 = \frac{1}{N_s}\sum_{n=0}^{N_s-1} s_{k,r}^2[n] = \frac{2N}{N_s}, \tag{19}$$

because in each of the N symbols in this interval, there are exactly 2 nonzero samples—the head and tail's first elements—with $s_{k,r}^2[n] = 1$, and the remaining samples in the symbol are 0. Substituting (19) into (18) gives

$$S_N\left(e^{j\omega}\right) = 2\bar{\sigma}_N^2\left[\frac{1}{N}\sum_{i=1}^{N}\sin^2\left(\frac{\omega H_i}{2}\right)\right]. \tag{20}$$

With $\bar{E}_N$ defined as the sample-average expectation operator, and H as the head-length sequence, (20) can be written as

$$S_N\left(e^{j\omega}\right) = 2\bar{\sigma}_N^2 \bar{E}_N\left[\sin^2\left(\frac{\omega H}{2}\right)\right]. \tag{21}$$

If the switching block's input is now assumed to be an ergodic random process such that the above sample averages converge to ensemble averages as $N \to \infty$, then the PSD of the switching sequence is

$$S\left(e^{j\omega}\right) = \lim_{N\to\infty} S_N\left(e^{j\omega}\right) = 2\sigma^2 E\left[\sin^2\left(\frac{\omega H}{2}\right)\right], \tag{22}$$

where E is the ensemble-average expected-value operator, $\sigma^2 = E\left[s_{k,r}^2[n]\right]$, and H is the head-length process.

The derivation above gives insight into the properties of the resulting PSD and the information required to compute it. The first-order shape of the switching sequence PSD is confirmed by (22). Additionally, it can be shown that the PSD is bounded in magnitude by 2 and has a continuous derivative that is likewise bounded in magnitude by 2. This result quantifies the smoothness of the PSD curve and implies that it is void of tones. It also follows from (22) that the curvature (*i.e.,* bandwidth) and signal-band area of the PSD are dictated by the statistics of the switching block input.

The previous analysis pertains to any switching block in the tree-structured DAC. To develop the DAC mismatch-noise PSD, this analysis is applied to each switching block in the tree-structured DAC. As previously noted, the $S_k(e^{j\omega})$ function in Section 3 is the PSD for each switching sequence in layer k. Therefore, (6) and (9) are equations of the form in (22). The functions $P_k(n,m)$ and p_n are used to obtain the head-length probabilities for the switching sequences in layers k ($k > 1$) and 1, respectively.

5. SECOND-ORDER ΔΣ MODEL

In Section 3, the expressions that are used to generate the DAC-noise PSD are functions of the statistics of the random symbol-type choices in the switching sequences and the behavior of the ΔΣ modulator output. For the analysis of the ΔΣ modulator output, it is assumed that the ΔΣ modulator has been operating for all time, or equivalently, has been started with random states in its integrators. In the second-order, analog ΔΣ modulator with a midscale input, the ΔΣ modulator output is a function of several noise sources including circuit noise, DAC mismatch noise, and quantization noise (the difference between the output and input of the quantizer). Therefore, obtaining the precise statistics of this output based on all of these noise sources is not practical, and a simplified model is required.

The simplified model is based on the assumption that the quantization noise determines the head-length probabilities and variances of the switching sequences, and the other noise sources have a negligible affect on these statistics. Because a midscale input corresponds to $x[n] = 0$, this assumption implies that the ΔΣ modulator output, $y[n]$ is the *quantization error*:

$$y[n] = e[n] - 2e[n-1] + e[n-2], \qquad (23)$$

where $e[n]$ is the quantization noise. This is a plausible assumption because the total power of the quantization error, across the entire spectrum, is much greater than the power contributed by the other noise sources in most ΔΣ modulator implementations.

For the analysis of $y[n]$ for $n \geq 0$, it follows from (23) that it is sufficient to determine $e[n]$ for $n \geq -2$. By the assumption described above, $e[n]$ can be expressed as

$$e[n] = \frac{1}{2} - \left\langle \frac{1}{2} - 2e[n-1] + e[n-2] \right\rangle, \qquad (24)$$

where $\langle\cdot\rangle$ is the fractional-part function. To solve this nonlinear difference equation, the samples $e[-2]$ and $e[-1]$ are required. It is shown in [5] that the quantization-noise samples in this ΔΣ modulator are uniformly distributed and pairwise independent. From this result, it follows that $e[-2] = \varepsilon_1$ and $e[-1] = \varepsilon_2$, where ε_1 and ε_2 are independent random variables that are uniformly distributed over the interval $(-1/2, 1/2)$. Given these initial random variables and (24), it can be shown by induction that

$$e[n] = \frac{1}{2} - \left\langle (n+1)(\varepsilon_1 - \varepsilon_2) + \left(\frac{1}{2} - \varepsilon_2\right) \right\rangle. \qquad (25)$$

Thus, the ΔΣ modulator output is a nonlinear function of two independent, uniformly distributed random variables.

Let $\hat{y}[n]$ be the difference between $y[n]$ and the DAC's midscale value: $\hat{y}[n] = y[n] - 2^{b-1}$, where b is the number of layers in the DAC. It can be shown with (25) that $\hat{y}[n]$ has the following properties:

- $\hat{y}[n] \in \{-1, 0, 1\}$.
- Alternating Property:
  If $\hat{y}[n] = \pm 1$, and the next nonzero value in this sequence occurs at the *l-th* sample, then $\hat{y}[l] = \mp 1$.
- Symmetry Property #1:
$$P(\hat{y}[m] = y_m : 0 \leq m < n) = P(\hat{y}[m] = -y_m : 0 \leq m < n),$$
  where P is the probability function and each y_m is an integer.
- Symmetry Property #2:
$$P(\hat{y}[m] = y_m : 0 \leq m < n) = P(\hat{y}[m] = y_{n-1-m} : 0 \leq m < n).$$

Let $\hat{x}_{k,r}[n] = x_{k,r}[n] - 2^{k-1}$, which is the difference between $x_{k,r}[n]$ and its midscale value. It can be shown that each $\hat{x}_{k,r}[n]$ sequence also possesses the properties listed above. This is a consequence of the operation of the switching blocks. With these properties, the functions $P_k(n,m)$ and p_n in Section 3 can be shown to produce the desired switching sequence statistics.

REFERENCES

1. AK2700: "High Precision, High Speed ADC: 16-Bits, 2.5MSPS," Product Data Sheet, Asahi Kasei Microsystems; Mar. 2000.
2. AD9260: "High-Speed Oversampling CMOS ADC with 16-Bit Resolution at a 2.5 MHz Output Word Rate," Product Data Sheet, Analog Devices, Inc.; Rev. B, 2000.
3. E. Fogleman, I. Galton, W. Huff, H. Jensen, "A 3.3V Single-Poly CMOS Audio ADC Delta-Sigma Modulator with 98dB Peak SINAD and 105-dB Peak SFDR," *IEEE Journal of Solid State Circuits,* vol.35, no.3, pp.297-307, March 2000.
4. I. Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 44, no. 10, pp. 808-817, Oct. 1997.
5. I. Galton, "Granular Quantization Noise in a Class of Delta-Sigma Modulators," *IEEE Transactions on Information Theory,* vol.40, no.3, pp.848-859, May 1994.