A NOVEL HIGHLY STABLE HIGH-RESOLUTION OVERSAMPLED Σ-Δ A/D CONVERTER CONFIGURATION

Neil A. Fraser and Behrouz Nowrouzian

Department of Electrical and Computer Engineering
University of Alberta
Edmonton, Alberta Canada

ABSTRACT

Feedforward and multiple-feedback Σ-Δ A/D converters offer high-resolution, but are susceptible to instability in the presence of capacitor tolerances in a corresponding switched-capacitor (SC) hardware implementation. The hitherto Σ-Δ A/D converters are usually based on, a) complementary signal and noise transfer functions, and/or b) unit-circle noise transfer function zeros. This paper is concerned with the development of a novel Σ-Δ A/D converter having, instead, magnitude-squared or magnitude complementary signal and noise transfer functions. The proposed A/D converter exhibits resolution and dynamic range properties similar to those of the existing feedforward and multiple-feedback A/D converters, but offers increased stability performance in the presence of capacitor tolerances in the SC hardware implementation. In addition, the SC hardware implementation of the resulting A/D converter leads to a capacitance spread which is comparable to that of hitherto Σ- Δ A/D converters.

1. INTRODUCTION

Recently, feedforward and multiple-feedback oversampled Σ-Δ A/D converters have found widespread use in digital signal processing applications [1]. Typical examples include the cascade-of-resonators (COR) [2], the cascade-of-integrators (COI) [3], and their combination, namely the cascade-of-resonators/integrators (CRI) [4] Σ-Δ A/D converters. A generic Σ-Δ A/D converter is shown in Fig. 1, where $U(z)$ represents the z-transformed input signal, and where $Y(z)$ represents the z-transformed output signal. In design situations, the constituent quantizer is usually replaced by a uniformly distributed additive white noise source $E(z)$. Then, the A/D converter may be characterized by the signal transfer function $STF(z)$ and the noise transfer function $NTF(z)$ in accordance with

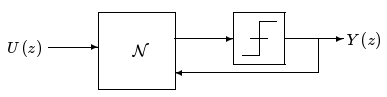

Fig. 1. Generic Σ-Δ A/D Converter Configuration

$$STF(z) = \frac{Y(z)}{U(z)} \equiv \frac{S(z)}{D(z)}, \tag{1}$$

$$NTF(z) = \frac{Y(z)}{E(z)} \equiv \frac{N(z)}{D(z)}, \tag{2}$$

where $D(z)$ represents the denominator polynomial common to both $STF(z)$ and $NTF(z)$, and where $S(z)$ and $D(z)$ represent the numerator polynomials of $STF(z)$ and $NTF(z)$, respectively.

Recently [5], a novel highly stable high-resolution oversampled Σ-Δ A/D converter configuration (MCOR) was developed, realizing magnitude-squared complementary or magnitude complementary signal and noise transfer functions. An empirical investigation of the corresponding (discrete) switched-capacitor (SC) hardware implementation of the proposed Σ-Δ A/D converter configuration demonstrated that it exhibits a superior level of stability in the presence of capacitor tolerances as compared to that of hitherto feedforward and multiple-feedback A/D converters. Furthermore, despite the apparent increase in stability, the achievable $SQNR$ remained comparable to that of hitherto feedforward and multiple-feedback A/D converters.

The present paper is concerned with the development of a new highly stable high-resolution Σ-Δ A/D converter featuring magnitude-squared or magnitude complementary signal and noise transfer functions. The resulting A/D converter possesses three important practical advantages as compared to the hitherto feedforward and multiple-feedback A/D converters, including a) its noise transfer function can be obtained without recourse to numerical optimization, (simplifying the design process), b) its noise transfer function is guaranteed to be bounded below 1, resulting in highly stable A/D converter operation, and c) in the signal band, where the magnitude of the signal transfer function is 1, the magnitude of the noise transfer function is automatically 0 resulting in high signal-to-quantization-noise ratio ($SQNR$) in an actual (nonlinear) converter operation.

Section 2 presents a synthesis method for the realization of magnitude-squared or magnitude complementary signal and noise transfer functions $STF(z)$ and $NTF(z)$ compatible with the proposed Σ-Δ A/D converter configuration. Section 3 presents an empirical investigation and Monte-Carlo simulation of the resulting Σ-Δ A/D converter for a corresponding SC hardware implementation. A comparison of the achievable $SQNR$ of the proposed A/D converter

and hitherto feedforward and multiple-feedback Σ-Δ A/D converters will demonstrate the superior stability performance in the presence of capacitor tolerances exhibited by the proposed configuration. Finally, the main conclusions of the paper are given in Section 4.

2. THE DEVELOPMENT OF THE PROPOSED CONFIGURATION

A pair of magnitude-squared complementary transfer functions $H_A(z)$ and $H_B(z)$ may be formed in accordance with [6], [7]

$$H_A(z) = \frac{1}{2}\left[H_1(z) - H_2(z)\right] \tag{3}$$

$$H_B(z) = \frac{1}{2}\left[H_1(z) + H_2(z)\right] \tag{4}$$

where $H_1(z)$ and $H_2(z)$ are a pair of all-pass transfer functions in accordance with [6], [7]

$$H_1(z) = \frac{1 - \frac{Z_1(z)}{R}}{1 + \frac{Z_1(z)}{R}}, \quad H_2(z) = \frac{1 - \frac{Z_2(z)}{R}}{1 + \frac{Z_2(z)}{R}} \tag{5}$$

where $\frac{Z_1(z)}{R}$ and $Z_2(z)R$ are a pair of (normalized) discrete-time reactance functions as obtained in the following.

Let us consider a rational transfer function $H(z)$ of order N, where N is odd for lowpass (or highpass) $H(z)$, and where N is even for bandpass (or bandstop) $H(z)$. Moreover, let $H(z)$ satisfy a relationship of the form [6], [7]

$$4H(z)H(z^{-1}) = \frac{1}{1 - \left[\frac{P(z)}{Q(z)}\right]^2} \tag{6}$$

where $P(z)$ is an antisymmetric polynomial, and $Q(z)$ is a symmetric polynomial in z. In addition, let z_{1i_1} (for $i_1 = 1, 2, \cdots, n_1$) denote those roots of

$$P(z) + Q(z) = 0, \tag{7}$$

which are inside the unit circle, and let z_{2i_2} (for $i_2 = 1, 2, \cdots, n_2 = N - n_1$) denote those roots which are outside the unit circle. Then, form the polynomials $P_1(z)$, $Q_1(z)$, and $P_2(z)$, $Q_2(z)$ in accordance with

$$P_1(z) + Q_1(z) = \prod_{i_1=1}^{n_1} (z - z_{1i_1}) \tag{8}$$

and

$$P_2(z) + Q_2(z) = \prod_{i_2=1}^{n_2} (z - z_{2i_2}^{-1}) \tag{9}$$

where $P_1(z)$, $P_2(z)$ are antisymmetric polynomials, and $Q_1(z)$, $Q_2(z)$ are symmetric polynomials in z. Then

$$\frac{Z_1(z)}{R} = \frac{\prod_{i_1=1}^{n_1}(z - z_{i_1 1}) - z^{n_1}\prod_{i_1=1}^{n_1}(z^{-1} - z_{i_1 1})}{\prod_{i_1=1}^{n_1}(z - z_{i_1 1}) + z^{n_1}\prod_{i_1=1}^{n_1}(z^{-1} - z_{i_1 1})} \tag{10}$$

$$\frac{Z_2(z)}{R} = \frac{\prod_{i_2=1}^{n_2}(z - z_{i_2 2}^{-1}) + z^{n_2}\prod_{i_2=1}^{n_2}(z^{-1} - z_{i_2 2}^{-1})}{\prod_{i_2=1}^{n_2}(z - z_{i_2 2}^{-1}) - z^{n_2}\prod_{i_2=1}^{n_2}(z^{-1} - z_{i_2 2}^{-1})}. \tag{11}$$

In this way, having determined the magnitude-squared complementary transfer functions $H_A(z)$ and $H_B(z)$ in terms of $H_1(z)$ and $H_2(z)$ (c.f. Eqns. 3 and 4), it is a simple matter to obtain a corresponding pair of magnitude complementary transfer functions $\tilde{H}_A(z)$ and $\tilde{H}_B(z)$ in accordance with

$$\tilde{H}_A(z) = H_A(z)^2, \qquad \tilde{H}_B(z) = H_B(z)^2. \tag{12}$$

Then, the signal transfer and noise transfer functions may be obtained as

$$STF(z) = H_A(z)\ (or \tilde{H}_A(z)), \tag{13}$$

$$NTF(z) = H_B(z)\ (or \tilde{H}_B(z)). \tag{14}$$

The resulting signal and noise transfer functions may be decomposed into $N(z)$, $D(z)$, and $S(z)$ in accordance with Eqns. 1 and 2.

It is expedient to recast the polynomial $D(z)$ in the form

$$D(z) = \mathcal{Z}'\mathcal{D}, \tag{15}$$

and the polynomials $N(z)$ and $S(z)$ in the forms

$$N(z) = \mathcal{Z}'\mathcal{N}, \tag{16}$$

$$S(z) = \mathcal{Z}'\mathcal{S}, \tag{17}$$

where $\mathcal{Z}' = [z^0, z^{-1}, z^{-2}, \cdots, z^{-N}]$, where $\mathcal{D}$, $\mathcal{N}$, and $\mathcal{S}$ are column vectors of length $N+1$ whose entries depend on the system parameters of the Σ-Δ A/D converter, and where N is the order of the A/D converter.

In the hitherto feedforward and multiple-feedback Σ-Δ A/D converters, the configuration proper imposes two restricting conditions on the signal and noise transfer functions, namely 1) the z^0 coefficient of $S(z)$ must be zero and 2) the z^0 coefficient of $N(z)$ must be unity. However, magnitude-squared or magnitude complementary signal and noise transfer functions require that the z^0 coefficient of $S(z)$ be non-zero and that the z^0 coefficient of $N(z)$ be unconstrained. To circumvent these two problems, consider the proposed Σ-Δ A/D converter as shown in Fig. 2 [1]. An analysis of this A/D converter reveals that

$$N(z) = \frac{G}{z^N}\left[(z-1)^N - \sum_{i=1}^{N} A_i(z-1)^{N-i}\right]. \tag{18}$$

Evidently, the parameter G corresponds directly to the z^0 coefficient of $N(z)$. It is convenient to let

$$\mathcal{A} = [1\ A_1\ A_2 \cdots A_N],$$
$$\mathcal{B} = [1\ B_1\ B_2 \cdots B_N],$$
$$\mathcal{R} = [R_1\ R_2 \cdots R_{N+1}].$$

Then it may be shown that

$$\mathcal{N} = \mathcal{C}_{MCOI1}\mathcal{A}G, \tag{19}$$

$$\mathcal{D} = \mathcal{C}_{MCOI2}\mathcal{B}, \tag{20}$$

$$\mathcal{S} = \mathcal{C}_{MCOI3}\mathcal{R}G, \tag{21}$$

[1] This A/D converter is an adaptation of the COI Σ-Δ A/D converter.

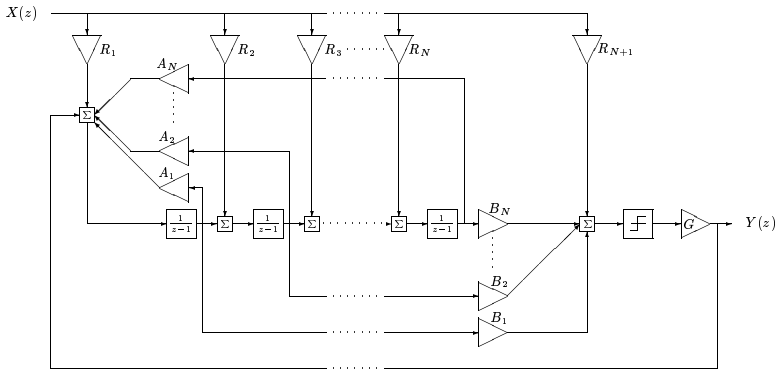

Fig. 2. Proposed Σ-Δ A/D Converter Configuration

where, for an Nth order A/D converter, $\mathcal{C}_{MCOI1}$ is a lower triangular matrix of order $N+1$ whose elements are independent of the A multiplier coefficients, $\mathcal{C}_{MCOI2}$ is a lower triangular matrix of order $N+1$ whose elements depend solely on the A and G multiplier coefficients, and $\mathcal{C}_{MCOI3}$ is a matrix of order $N+1$ whose elements are solely dependent on the A and B multiplier coefficients. In the case of $N=3$, for example,

$$\mathcal{C}_{MCOI1} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3 & -1 & 0 & 0 \\ 3 & 2 & -1 & 0 \\ -1 & -1 & 1 & -1 \end{bmatrix} \tag{22}$$

$$\mathcal{C}_{MCOI2} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3-A_1 & -G & 0 & 0 \\ 3+2A_1-A_2 & 2G & -G & 0 \\ -1-A_1+A_2-A_3 & -G & G & -G \end{bmatrix} \tag{23}$$

$$\mathcal{C}_{MCOI3} = \left[\begin{array}{lll|l} 0 & 0 & 0 & \\ B_1 & B_2 & B_3 & \\ 2B_1+B_2 & B_3-B_2(2+A_1)+B_1A_2 & -B_3(2-A_1)+B_1A_3 & \mathcal{C}_{\cdot 1} \\ B_1-B_2+B_3 & -B_3(1+A_1)+B_2(1+A_1)+B_1(A_3-A_2) & B_3(1-A_2+A_1)+B_2A_3+B_1A_3 & \end{array}\right] \tag{24}$$

where $\mathcal{C}_{\cdot 1}$ represents the first column of the matrix $\mathcal{C}_{MCOI2}$.

In this way, once $\mathcal{N}$, $\mathcal{D}$, and $\mathcal{S}$ have been obtained, the coefficient G may be obtained from $\mathcal{N}$, and the multiplier coefficients, $\mathcal{A}$, $\mathcal{B}$, and $\mathcal{R}$ may be obtained through the inversion of Eqns. 19, 20, and 21, respectively.

3. EMPIRICAL INVESTIGATION OF THE PROPOSED Σ-Δ A/D CONVERTER CONFIGURATION

This section is concerned with a demonstration of the main salient features of the proposed Σ-Δ A/D converter configuration in a corresponding (discrete) SC hardware implementation [2]. It is shown that the resulting SC hardware implementation exhibits a high degree of stability in the presence of capacitor tolerances, and, in addition, leads to an achievable $SQNR$ comparable to those of the hitherto feedforward and multiple-feedback A/D converters.

By employing the procedure given in [5], a 5'th order, 16× oversampled, magnitude-squared complementary Σ-Δ A/D converter with a $SQNR$ of 55 dB was designed. As described in the previous section, the multiplier coefficients were determined and are as shown in Table 1. The dependence of the achievable $SQNR$ as a function of DC input signal amplitude was determined, leading to the results shown in Fig. 3. These results indicate a maximum achievable $SQNR$ of 53.6 dB with a DC input signal amplitude of -6.02 dB, which is comparable to the results obtained for the COR A/D converter in [8] (satisfying similar design specifications) [3].

Table 1. Nominal Multiplier Values

R_1	0.85439	R_2	3.33027	R_3	-39.89807
R_4	135.39195	R_5	-23.34846	R_6	.04863
B_1	-0.88093	B_2	-0.30574	B_3	-0.09522
B_4	-0.01451	B_5	-0.00150		
A_1	-0.05428	A_2	-0.05491	A_3	-0.00127
A_4	-0.00064	A_5	0	G	0.72452

The capacitor values of the SC hardware implementation were scaled for maximum dynamic range and for minimum capacitance using the method described in [9]. This led to a a total capacitance of 235.5 units (in a single ended configuration) and a capacitance spread of 42.05 (comparable to the spread of 30.76 in [2] for a fourth-order COR A/D converter). Monte-Carlo simulations on 1000 different samples of the magnitude-squared complementary Σ-Δ A/D converter led to the determination of the actual $SQNR$s as shown in Fig. 4 and summarized in Table 2, where the capacitor values were individually perturbed around their

[2] This implementation uses the COI SC circuit with the addition of $N+1$ capacitors to implement the coefficients of $\mathcal{R}$ and is not shown here due to the limited space.

[3] The $SQNR$ was 61.1 dB with a DC input signal amplitude of -8 dB.

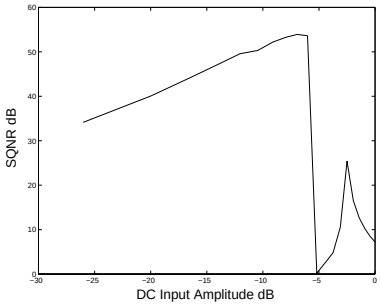

Fig. 3. SQNR as a Function of DC Input Signal Amplitude

nominal values with a Gaussian distributed white random variable ϵ of zero mean and a standard deviation of 0.00333 leading to maximum perturbation $\epsilon_{max} = 1\%$ [4]. This led

Table 2. SQNR Statistics with $\epsilon_{max} = 1\%$

Nominal	53.6 dB	Max	68.8 dB
Variance	.796 dB	Min	49.1 dB
Mean	53.6 dB		

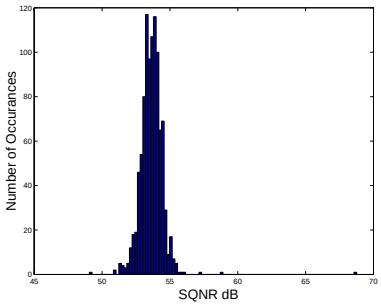

Fig. 4. Monte-Carlo Simulation Results for $\epsilon = 1\%$

to the determination of the percentage of unstable Monte-Carlo samples for various values of ϵ_{max} as shown in Table 3, where the values for the MCOR A/D converter were obtained in [5], and where the values for the COR, COI, and CRI A/D converters were obtained in [8]. As is evident,

Table 3. Percentage of Unstable Monte-Carlo Samples

ϵ_{max} (%)	.1	.5	1	1.5	2
Proposed: % Unstable	.2	.2	.8	4.5	12.4
MCOR: % Unstable	.1	.2	1.8	7	24.1
COR: % Unstable	18.4	22.0	24.9	33.3	39.4
COI: % Unstable	16.6	24.7	37.4	43.7	51.8
CRI: % Unstable	23.4	25.0	28.4	36.2	42.3

the proposed Σ-Δ A/D converter shows a high degree of stability (particularly at small values of ϵ_{max}) compared to the COR, COI, and CRI A/D converters. The proposed A/D converter is comparable to the MCOR A/D converter at low capacitor tolerances and shows less stability problems at large capacitor tolerances.

[4]The samples with substantially low SQNR imply unstable Σ-Δ A/D converter operation and were discarded.

4. CONCLUSION

This paper has presented a novel highly stable high-resolution oversampled Σ-Δ A/D converter configuration, realizing magnitude-squared complementary or magnitude complementary signal and noise transfer functions. Empirical investigation of a corresponding (discrete) SC hardware implementation of the proposed Σ-Δ A/D converter configuration has demonstrated that the A/D converter exhibits a superior level of stability in the presence of capacitor tolerances as compared to that of hitherto feedforward and multiple-feedback A/D converters. It has further been demonstrated that the proposed A/D converter provides better stability performance at high capacitor tolerances as compared to the MCOR A/D converter. Furthermore, despite this increased stability, the achievable $SQNR$ remains comparable to that of hitherto feedforward and multiple-feedback A/D converters.

5. ACKNOWLEDGEMENTS

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