HIGH-SPEED CORDIC IMPLEMENTATIONS USING ADVANCED CIRCUIT TECHNIQUES

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ABSTRACT

This paper presents results on using advanced domino circuit design techniques to implement a CORDIC processor. Skew-tolerant domino, enhanced precharged contention, non-blocking domino and pulsed reset domino circuit techniques are explained and applied to the implementation of this functional unit. For comparison purposes, a baseline design using standard two-phase domino with intermediate latches is also developed. Simulation results show that significant throughput improvement is possible using the advanced circuit techniques, with the pulsed reset style having the highest speed. On the other hand, these approaches result in increased power dissipation.

1. INTRODUCTION

CORDIC algorithms have been widely applied in many signal processing applications, including matrix eigenvalue and singular value decomposition calculations. In many of these applications, attaining the highest possible throughput is the primary design goal. The key computations consist of an iterative series of shifts and additions or subtractions. Signed digit approaches are well matched to this application, since the iterative calculations can be done in a carry-save manner. In this case, one also needs binary to signed digit and signed digit to binary converters at the beginning and end of the iterative loop.

In this paper, we will apply several recent advancements in domino CMOS circuit design to achieve very high speed operation in a CORDIC angle unit [1], [2]. Specifically, we will consider the following design styles: skew-tolerant domino [3], [4], [5] with enhanced precharge contention [6], non-blocking domino [7], [8], [9] and pulsed reset domino [10], [11]. As a baseline for comparison, we also consider a standard domino implementation using two-phase clocking with mid-cycle latches. We will present simulation results to show how these advanced circuit design approaches yield significant improvements in throughput, at the expense of increased power dissipation.

2. CORDIC ANGLE UNIT

The iterative computations can be done in a carry-save manner using signed digit adders in the constant-factor redundant CORDIC algorithm [1]. For the angle calculation in vectoring mode, the angle $\theta = tan^{-1}(Y_a[0]/X_a[0])$ is obtained to n-bit precision from a quantity $Z_a[n]$ using the following recurrence equations (with $Z_a[0] = 0$):

$$X_a[i+1] = X_a[i] + \sigma_i 2^{-i} Y_a[i] \quad (1)$$

$$Y_a[i+1] = Y_a[i] - \sigma_i 2^{-i} X_a[i] \quad (2)$$

$$Z_a[i+1] = Z_a[i] + \sigma_i tan^{-1} 2^{-i} \quad (3)$$

$$\sigma_i = \begin{cases} +1 & if \quad Y_a[i] \geq 0 \\ -1 & if \quad Y_a[i] < 0 \end{cases} \quad (4)$$

In the above equation, σ_i represents the direction of rotation at step i of the iterative loop. A block diagram corresponding to Equations (1) and (2) is shown in Figure 1.

3. HIGH-SPEED CIRCUIT TECHNIQUES

3.1. Skew-Tolerant Domino with Enhanced Precharge Contention

Skew-tolerant domino is based on the use of overlapping multi-phase clocks [3], [4], [5]. The overlap time between adjacent phases eliminates the need for intermediate latches. In addition, it provides an efficient method to budget for a certain degree of imbalanced logic and clock skew between the blocks. For example, consider two adjacent blocks of domino logic, one clocked on ϕ_i and the other clocked on ϕ_{i+1}. The interval when both clocks are high is the time

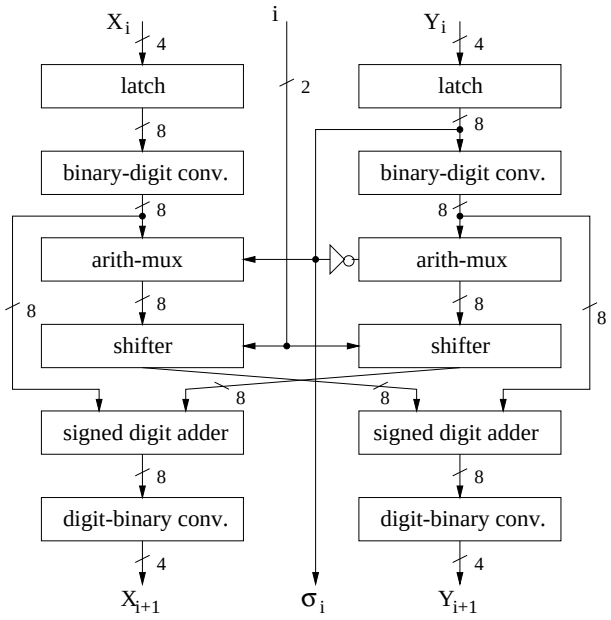

Fig. 1. Block diagram for the constant-factor redundant CORDIC angle unit.

when circuits that are clocked on ϕ_i can borrow time from the subsequent circuits that are clocked on ϕ_{i+1}. These effects lead to a significant reduction in the amount of clocking overhead compared to standard two-phase domino. The net result is that the circuits can operate at higher speed.

Enhanced precharge contention (EPC) [6] also provides increased computational efficiency by allowing useful work to be done during the precharge phase. The basic idea is to remove the NMOS evaluate or "foot" transistors from the pull down network, so that intentional fighting occurs during the precharge phase. This fighting is beneficial in the sense that it reduces the precharge voltage on those nodes that will eventually be discharged to ground during the subsequent evaluate phase. With a reduced precharge voltage, it will take a shorter amount of time to discharge those nodes, which increases the speed of the signal propagation. While the technique does dissipate DC power along the paths that are fighting, this may be considered to be an acceptable trade-off in high-speed applications.

3.2. Non-Blocking Domino

A domino logic stage will have one or more inputs. In general these inputs can arrive at the stage at different times. If the clock phase controlling a stage is high, the latest arriving input signal will determine the worst-case time when the stage will evaluate. A clocking scheme is said to be non-blocking if, for all domino stages, the rising edge of the clock phase controlling a stage occurs before the latest input signal arrives [7], [8], [9]. If this is not the case, then the clocking scheme is said to be blocking. The two cases are illustrated in Figure 2, where x is the latest arriving signal into a domino logic stage that is controlled by clock phase ϕ_i. In order to maximize the computation speed, one should design the critical path so that it consists of a series of non-blocking stages.

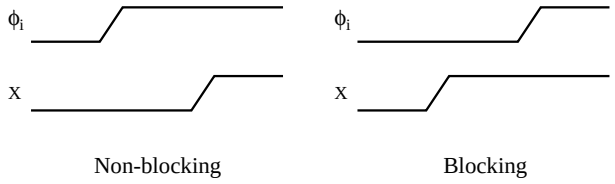

Fig. 2. Timing diagrams for non-blocking and blocking cases.

3.3. Pulsed Reset Domino

Another recently introduced high-speed circuit style is pulsed reset domino [10], [11]. An example of this circuit style is shown in Figure 3. The pulsed clock ϕ_p is 3 time units wide and the transistors are sized so that the delay through each static or dynamic logic gate is 1 time unit. The first domino stage evaluates at the rising edge of ϕ_p. 3 time units later, ϕ_p goes low and node 1 goes low, so the first domino stage precharges. The evaluation and precharge of the second and third stages are delayed by 2 and 4 time units, respectively. The circuit provides adequate margin for the local and global races associated with the output latch. Note that foot transistors are not required in the second and third stages.

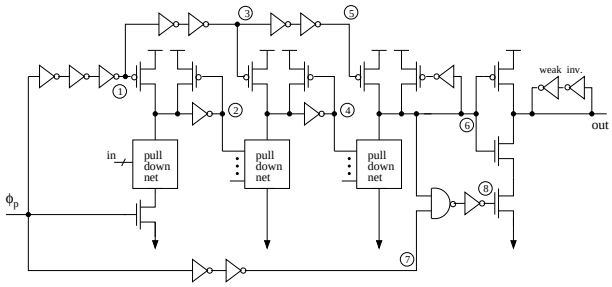

Fig. 3. Circuit structure for pulsed reset domino.

4. PERFORMANCE RESULTS AND COMPARISONS

In order to determine the relative merits of these advanced circuit techniques, we performed HSPICE simulations using the 0.25 micron TSMC process with a supply voltage of 3.3V. We used skewed static gates at the outputs of domino stages to improve the evaluation times and secondary precharge

transistors at internal nodes in pull-down networks to control charge sharing. Weak PMOS keepers were included for improved robustness against noise.

As a baseline for comparison, we simulated the CORDIC angle unit using standard two-phase domino, with mid-cycle latches placed between the shifter and the signed digit adder blocks. The results for this case are shown in Figure 4. One can see that the clock cycle time is 2.76 ns and several sources of overhead are evident. There are two latch propagation times and there is unused or "dead" time during the first half-cycle. The dead time is due to the imbalance in the propagation delays during the two half-cycles. These sources of overhead are typical of the situation one encounters in standard two-phase domino designs.

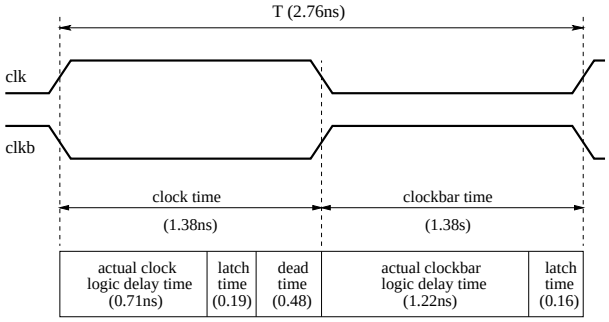

Fig. 4. Simulation results for traditional two-phase clocking with mid-cycle latches.

The results for skew-tolerant domino with 4-phase overlapping clocks and enhanced precharge contention are shown in Figure 5. The partitioning of the logic into each of the four clock phases is shown in the figure. Note that there are no latch propagation delays since latches are not required when overlapping clock phases are used. The cycle time is reduced to 1.84 ns, and there is one instance of time borrowing and two instances of enhanced precharge contention.

The results for the non-blocking domino design are shown in Figure 6. The phases ϕ_1 and ϕ_2 are delayed from the clock ϕ that drives the source latches, and phase ϕ_3 is delayed and stretched to meet the hold time requirement of the destination storage elements. Note that the propagation delay time is further reduced to 1.77 ns. The improvement is due to the fact that no critical signal waits for a clock phase to go high. While the EPC in the previous case allows some useful work to be done during precharge, it is not as effective as simply allowing the critical signal to propagate through directly.

Finally, Figure 7 shows the simulation results for the case of pulsed reset domino. As shown, the propagation delay is reduced even further to 1.51 ns. The speed increase over the non-blocking design is due to the fact that the pulsed reset circuits do not use evaluate transistors in the pull-down networks after the first stage of logic.

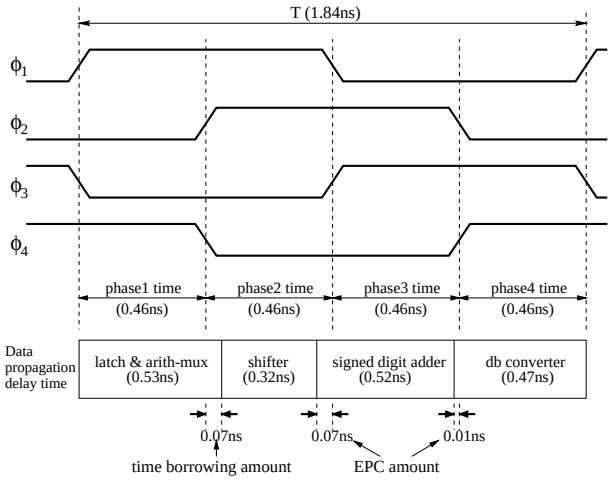

Fig. 5. Simulation results for skew-tolerant domino with enhanced precharge contention.

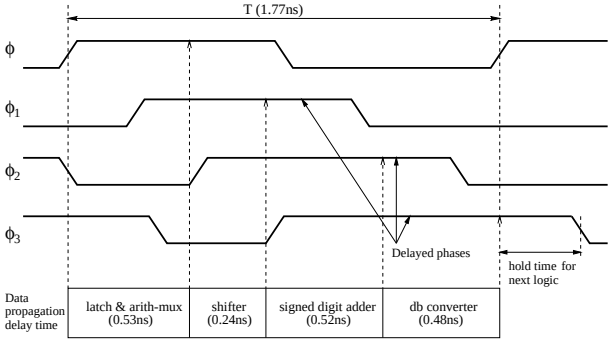

Fig. 6. Simulation results for non-blocking domino.

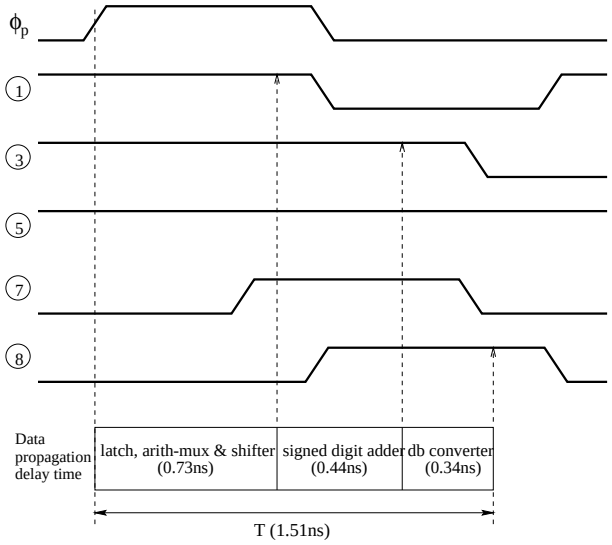

Fig. 7. Simulation results for pulsed reset domino.

The propagation delays for all four implementations of the CORDIC angle unit are summarized in Table 1. It is evident that all three of the advanced circuit techniques are substantially faster than the baseline implementation, with the pulsed reset design being the fastest.

Table1: Propagation delay comparisons.

High-speed circuit technique	Propagation delay time	Improvement
Traditional 2 phase clocking	2.76 ns	- - -
4 phase overlapping clocks with EPC	1.84 ns	33.3 %
Non-blocking domino	1.77 ns	35.9 %
Pulsed reset domino	1.51 ns	45.3 %

The average power dissipation during the propagation delay time for each of the circuit design styles is given in Table 2. In order to provide a fair comparison, the circuits required to generate the local clock phases in each case are included in the power results. Each of the advanced circuit techniques uses more power than the baseline design, with the pulsed reset implementation requiring the highest power.

Table2: Power consumption comparisons.

High-speed circuit technique	Average power	Increase
Traditional 2 phase clocking	115.4 mW	- - -
4 phase overlapping clocks with EPC	263.2 mW	128 %
Non-blocking domino	234.3 mW	103 %
Pulsed reset domino	439.9 mW	281 %

5. CONCLUSIONS

We have presented advanced circuit design techniques and simulation results for high-speed implementations of a constant-factor redundant CORDIC angle unit. The relative benefits of skew-tolerant domino with enhanced precharge contention, non-blocking domino and pulsed reset domino were explained and quantitatively demonstrated. Each of the three advanced circuit implementations is substantially faster than a baseline design using two-phase domino circuits with intermediate latches. The pulsed reset domino implementation resulted in the highest performance of all of the design implementations. At the same time, these circuit techniques result in higher power dissipation, so they may not be appropriate for applications in which low power consumption is the primary design objective.

6. REFERENCES

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