A SIMPLE, NON-INVASIVE PROBE FOR RECONSTRUCTING SIGNALS INSIDE A DSP

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ABSTRACT

A simple, non-invasive probe is proposed that extracts digital samples of a signal of interest from a DSP and reconstructs the samples into an equivalent analog signal. The probe is useful for software design and debugging as well as troubleshooting and verification of DSP systems in the field. A sample buffering system ensures that the digital samples are reconstructed into analog samples at substantially constant intervals, even if the DSP generates the digital samples at varying intervals. The buffering system uses a control loop to generate the analog samples at a sample rate that is equivalent to the mean sample rate of the digital samples. Consequently, the reconstructed analog signal accurately represents the digital signal found within the DSP. This signal may then be sent to conventional test equipment suited for analysis of analog signals. Details beyond the scope of this paper may be found at http://eepatents.com/probe.

1. INTRODUCTION

1.1 Background of the Problem

The signals generated by the modern DSP have become increasingly complex and difficult to analyze. For proper development and testing of the DSP's sophisticated algorithms, the digital signals should be analyzed in real-time operation. A "Boundary Scan" capability is needed for digital signals inside a DSP, analogous to the design-for-test capability that the IEEE 1149.1 concept offers for digital IC design.

Digital signals inside a DSP could be reviewed and analyzed using conventional test equipment if an analog reconstruction could be extracted from the DSP using a simple "Boundary Scan" signal probe. Such a capability would allow conventional test equipment, including oscilloscopes, spectrum analyzers, and modulation analyzers, to be used for DSP design. An analog reconstruction is required because such equipment cannot process the raw processions of numbers that make up digital signals. The relationship between amplitude level and time is critical.

The DSP designer can obtain an analog approximation of a digital signal by transferring digital samples of the signal from the DSP to a D/A converter. This may be done by inserting a simple "probe" command into the portions of DSP code where such digital samples are produced. In many cases, however, the DSP algorithms produce the samples at widely varying intervals. The digital samples usually have lost their real-time relationship to the analog signal they represent. Consequently, accurate reconstruction of such samples often cannot be obtained by simply reconstructing each digital sample into an analog sample whenever it occurs.

The digital samples are produced at widely varying time intervals for a number of reasons, including the servicing of interrupts and high-level coding of the signal processing functions. In addition, modern DSPs often execute their algorithms in complex software structures having multiple threads. Further, some signal processing algorithms, such as the square root function, can take a varying amount of time to execute, and this execution time can depend on the amplitude of the input signal. In addition, multiple samples are often processed in bursts for greater efficiency. Algorithms processing such burst-mode signals produce several samples within a relatively narrow time interval.

Thus, sample timing is a fundamental problem with the reconstruction of digital signals from a DSP. The digital samples appear at intervals which are not known and which may vary widely from one sample to the next. For an accurate analog signal to be reconstructed, its samples must be spaced at relatively constant intervals. The true rate at which the digital samples are produced must be preserved, so that the analog signal accurately reconstructs the real-time signal represented by the digital samples.

1.2 Summary of the Proposed Solution

A simple, non-invasive probe [1] is proposed for extracting digital samples of a signal of interest from a DSP and accurately reconstructing them into an equivalent analog signal, even when the digital samples have lost their real-time relationship to the signal they represent. The probe includes a buffer that stores the samples from the DSP as they are extracted, no matter how much variation there is in the interval between such samples. The probe then reconstructs the digital samples into a series of uniformly spaced analog samples that accurately reproduce the equivalent analog signal. The spacing of the analog samples is substantially constant even when there is considerable variation in the time intervals between the digital samples extracted from the DSP.

The proposed probe makes a single serial connection to a conventional DSP. A simple "probe" command is inserted in the DSP code where a digital sample of a signal of interest is produced. The probe command sends each bit of the digital

sample to a special test port on the DSP, and consequently to the probe, in serial format.

The special test port may be an existing DSP serial port, in which case the probe command may be a single DSP instruction transferring the digital sample from a register to the port. However, the DSP designer need not reserve a dedicated serial port for connecting the probe to the DSP. An I/O pin may also be used as an asynchronous serial test port. The probe command then sends each bit of the digital sample to the I/O pin by executing a shifting function for a number of DSP cycles.

The DSP designer need not have any concern about when the digital samples are produced. The probe extracts the sample whenever it appears on the designated output port. The probe then reconstructs the digital samples into analog samples at the same mean rate at which the digital samples are produced, but with a constant interval between samples.

The proposed probe performs a reconstruction function for digital signals analogous to the function of a microprocessor disassembler. A microprocessor works with binary numbers that represent instructions, while a DSP works with binary numbers that represent analog signals. In the same way that a disassembler reconstructs binary numbers into microprocessor instructions, the proposed probe "disassembles" the DSP's binary representations of an analog signal into an accurate analog signal. Such a signal may be viewed and analyzed using an oscilloscope or other conventional test equipment.

2. HARDWARE

2.1 Sample Reconstruction Circuit

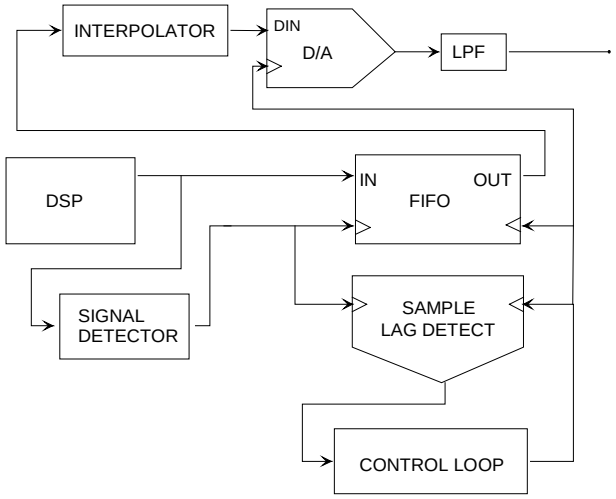

Figure 1. Block Diagram of the probe, showing the reconstruction circuit.

Figure 1 shows a block diagram of the probe, which includes a sampling buffering system and D/A converter. The sample buffering system may be implemented in a DSP (separate from the DSP being probed) and includes a control loop and a FIFO buffer memory. The control loop sets the interval between output samples from the FIFO to be equivalent to the mean interval between input samples. The control loop also ensures that the output sample interval is substantially constant, even if there is a great deal of variation between the input sample intervals.

The probe is connected to the DSP via a special test port on the DSP. The special test port may be one of the DSP's existing serial ports, using a three-wire synchronous format with dedicated framing and/or clock signals. Alternatively, one of the DSP's I/O pins may be used to create single-wire test port. The probe may be connected to such a port using a conventional oscilloscope probe.

Multiplexed signals may be sent to several probes via a single test port. In such a configuration, each probe is programmed to respond only to those digital samples that are produced by one of the multiplexed signals.

When the probe detects that the DSP has sent it a digital sample, it reads the sample into a FIFO buffer memory. A sample error counter is incremented when the sample is sent to the FIFO. When a sample is read from the FIFO, this sample error counter is decremented. Accordingly, the number of samples stored in the FIFO buffer memory corresponds to an error value. This error value is then fed to a control loop, which sets the rate at which samples are read from the FIFO.

The output samples read from the FIFO are reconstructed into an analog signal that accurately represents the digital signal found within the DSP. The output samples may be sent to an interpolator on their way to the D/A converter. Interpolation increases the sample rate, reducing alias distortion of the reconstructed output signal. The output signal is then sent to conventional test equipment suited for analysis of analog signals.

2.2 Physical Construction

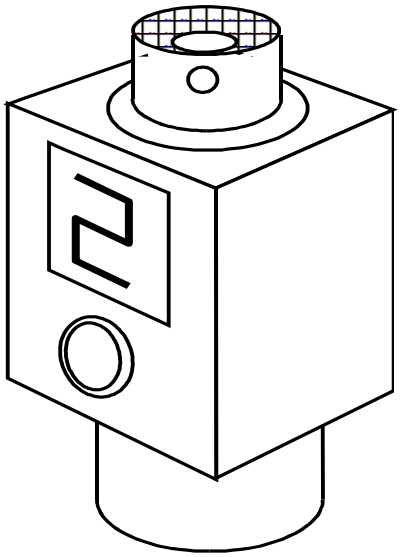

Figure 2. The probe designed as an oscilloscope probe adapter for digital signals.

Figure 2 above shows the probe designed as an adapter that allows a conventional oscilloscope to view signals within the DSP using its standard oscilloscope probe. The oscilloscope

probe makes a single-wire connection to a serial test port on the DSP. As discussed above, this test port may be a standard DSP serial port, or simply an I/O pin.

The oscilloscope probe connects to a standard BNC female connector on the adapter. The adapter has a standard BNC male connector on its other end for transmitting a reconstructed analog output signal to an oscilloscope or other analog test equipment. A selection button allows the user to select a single one of several multiplexed signals that may be present on the test port. Only samples produced by this selected signal are reconstructed into an analog signal on the output. The selected signal is identified with an LED or LCD indicator.

2.3 Sample Buffering System

The combination of the control loop with a FIFO and sample lag detector forms a sample buffering system. The control loop sets the output sample rate according to the sample lag between input and output samples stored in the FIFO. The output sample rate is preferably a linear function of this sample lag over time. Because input samples may arrive in bursts, the sample lag may have considerable variance. This variance needs to be greatly attenuated so that the interval between output samples is essentially constant.

The control loop uses an error term E, which is applied to the input of a loop filter. The filter is designed to have a lowpass response with a low cutoff frequency. The purpose of the loop filter is to ensure that the output sample rate has a substantially constant interval, even when bursts of samples give error term E substantial variance. Accordingly, the cutoff frequency of the filter should be made considerably lower than the rate at which bursts of samples are to be extracted.

A cutoff frequency (fc) of 0.0001 times the sample processing rate (fs) has been found desirable. An even lower cutoff frequency would be better for some applications if practical to implement. To realize such a low cutoff frequency with a DSP loop filter, an IIR lowpass filter should be used, with special consideration given to the effects of finite-precision arithmetic. A single-pole Butterworth lowpass filter with fc=0.0001*fs has been successfully implemented in a DSP control loop using 16-bit arithmetic.

The output of the loop filter is proportional to the time-averaged sample lag between input and output samples stored in the FIFO, as determined by the sample lag detector. The loop gain of the control loop is defined as the frequency step added to the output sample rate with one additional sample of error present on sample error E. When sample error E increases by this amount, the frequency of output sample clock C should increase by the value of the loop gain (A). A desirable value of loop gain has been found to be in the range from A = 5000 Hz/sample to A = 10,000 Hz/sample. Loop gains beyond this range seem to make the loop unstable and actually increase the settling time of the loop.

3. SIMULATION RESULTS

Matlab® simulation, as well as successful testing of a prototype, has shown the control loop to be effective for generating a steady reconstruction clock from bursts of input samples. The simulation shows reconstruction of sample bursts at a mean rate of 1,000,000 samples/sec. Although this sample rate is higher than the highest rate encountered in many applications, it allows easy visualization of the operation of the control loop within the sample buffering system. The simulation plots show the reconstructed output signal as it appears without an interpolator or lowpass filter on the output.

Figure 3 shows a burst of eight digital input samples. There is a great difference between the sample interval within the burst and the interval between bursts.

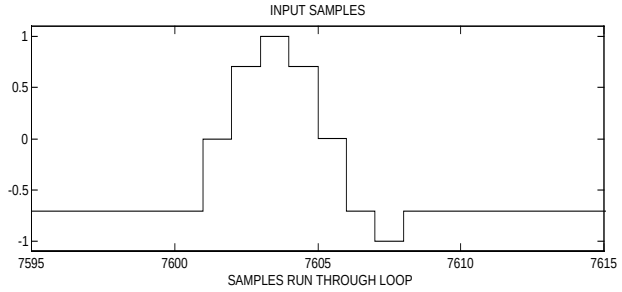

Figure 3. Analog levels represented by a burst of digital input samples entering the probe.

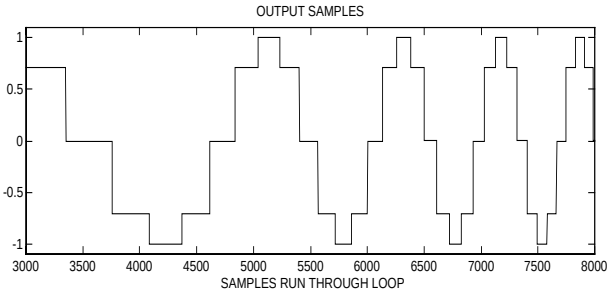

Figure 4. Analog output samples after repeated bursts of digital input samples.

Figure 4 shows the analog reconstruction of a signal represented by several of the digital sample bursts shown in Figure 3**.** The control loop "catches up" to the mean rate of the input samples and begins to send analog output samples at substantially constant intervals.

Figure 5 below shows two bursts of eight input samples plotted on the same time base as a reconstructed output signal. If the sequence of digital input samples shown in the upper plot were reconstructed without buffering, simply using the timing of the input samples as shown, the analog signal would of course be unrecognizable. The reconstructed analog output of the sample buffering system, shown in the lower plot of Figure 5, is easily recognized as a sampled sine wave.

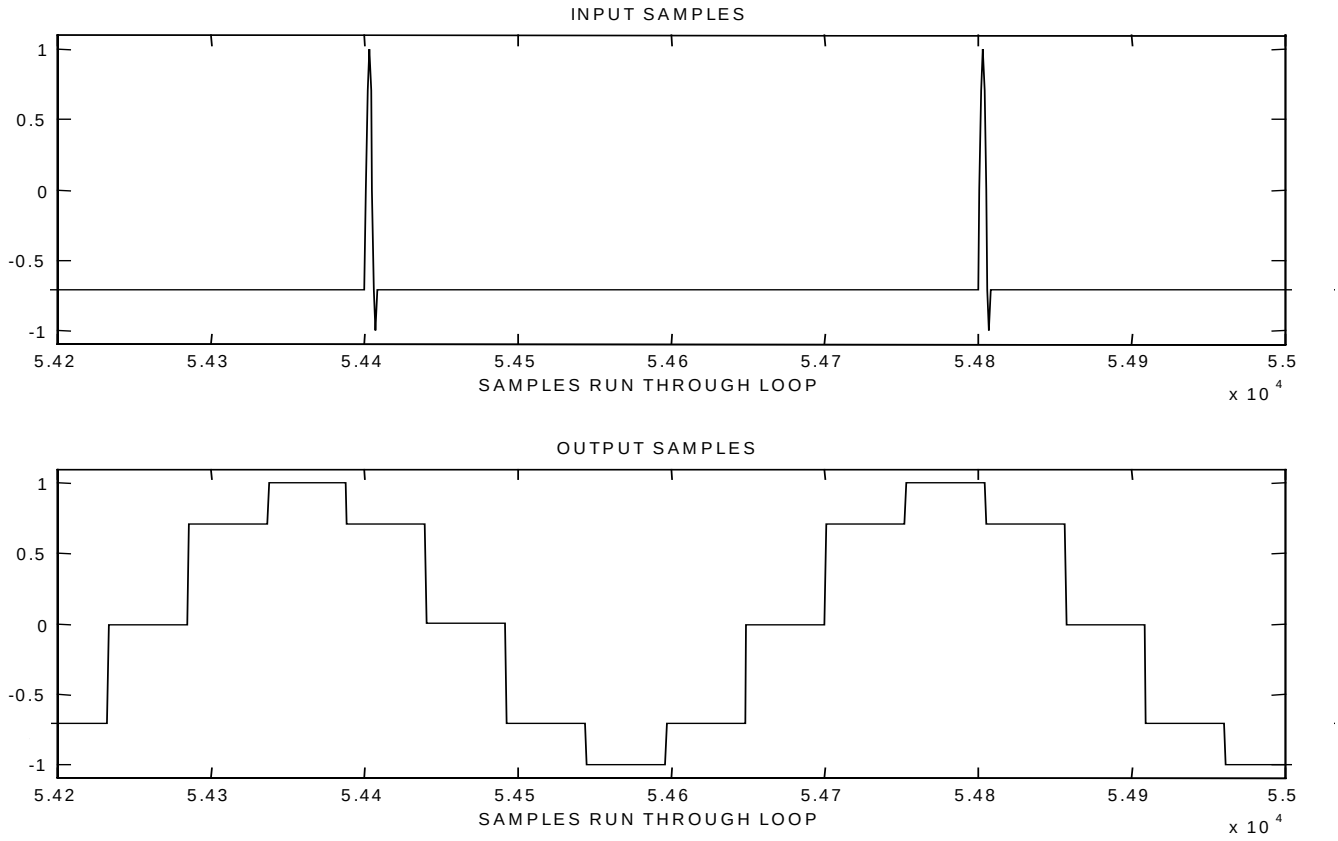

Figure 5. Input and output samples of the sample buffering system plotted on the same time base.

The upper plot of Figure 5 shows that two bursts of eight samples are received in the time interval occupied by a single period of the reconstructed sine wave. Each period of the sine wave contains 16 analog samples. The control loop in the simulated sample buffering system is setting the output sample rate to be substantially equal to the input sample rate while maintaining a substantially constant interval between output samples. This is significant in view of the tremendous difference between the time interval separating input samples within bursts and the time interval separating bursts.

Figure 6 is a long-term plot of the output sample rate of the simulated control loop. A complete transition to a steady-state reconstruction sample rate takes about 100,000 samples. This requires no more than a few seconds. Much more time than a few seconds is typically spent analyzing the signal, so this short transition time does not significantly impact the convenience that the probe offers in development and testing of DSP algorithms and systems.

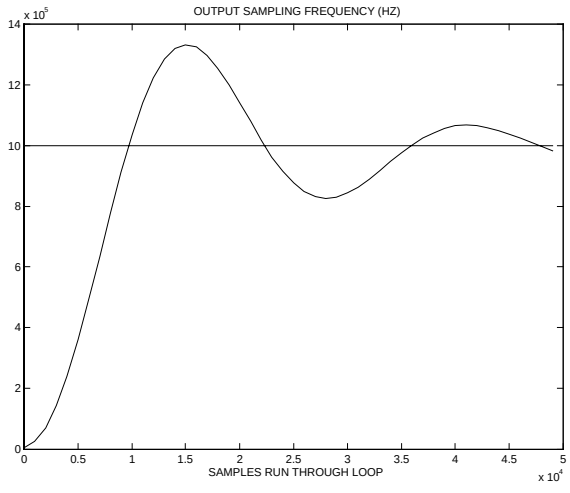

Figure 6. Long-term plot of the output sample rate of the simulated control loop.

4. REFERENCES

[1] Pending U.S. patent application of Edwin A. Suominen and Robert Roth. See http://eepatents.com/probe for detailed information.