CLOCK COMPENSATION IN A DATA/FAX RELAY SYSTEM

Ehsan Daeipour
DSP Software Engineering, Inc.
175 Middlesex Turnpike
Bedford, MA 01730
Ehsan@dspse.com

ABSTRACT

In Data/Fax relay applications, one challenge is to overcome problems associated with having independent clocks in the system. Due to slight differences in the clock frequency of the relay system compared to the far modems (fax machines), the relay system is unable to transmit with the same rate that it receives data. Eventually, the system either starves for data or loses data due to under/over flow of its buffers. The clock difference problem in a Demod/Remod system and a method to compensate for it is addressed in this paper. The transmitter clock in each side of the relay system is tuned to match with the clock rate at the other side. This clock tuning is done via a closed loop feedback system. The bit error rate measurements show a significant improvement in the performance of the Demod/Remod system when the clock difference is compensated.

1. INTRODUCTION

Transparent relay of Voice, Fax and Data (VFDR) over media with limited bandwidth is a new challenge in telecommunications industry. Many applications involve reliable transmission of voice, data, fax over digital wired or wireless channels. Examples of such applications are wireless local loop, satellite communication, Fax over internet, etc [1,2].

A well-designed Data/Fax Relay yields a minimal increase in transmission bandwidth compared to the data rate. One way to transparently relay fax/data is to apply conventional coding techniques used in encoding voice signal. However, such coding significantly deteriorate the signal quality. Reliable data transmission via conventional coding requires a bandwidth significantly larger than the actual data rates.

A bandwidth efficient method to relay Data/Fax, also named Demod/Remod system, involves demodulation of the incoming fax/data signals in one side and re-modulating them in the other side after transmitting through the digital channel. It is usually required that the relay system automatically detects and distinguishes between voice, fax and data signals and handle the proper application for each of them. Such a relay system for data/fax is depicted in Figure 1. The relay system presented in this paper is completely developed in DSP Software Engineering, Inc. on TMS320C3x and TMS320C54x DSP processors and is capable of transparent transmission of voice via G723 vocoders, group3 Fax, including V27ter, V29 and V17, and data including B103, V22bis and V32bis up to 14400 bps over a 16kbps channel. The additional bandwidth is used for transmission of control/status bits and additional spare bits due to clock difference as explained in Section 2.

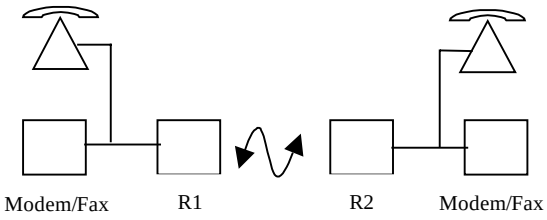

Figure 1: Voice, Fax, Data Relay (VFDR)

Challenges involved in a Demod/Remod system include, automatic detection of voice, fax and data and appropriate switching between them, proper handling of modem and fax protocols through the relay system, compensation for the clock difference between the relay system and far, etc. The focus of this paper is on the problems associated with the existence of independent clocks in the components of the Demod/Remod application and a new simple, though novel, solution for it. This issue and our approach is further described in Section 2. The results of experiments for the evaluation of the clock compensation approach are presented in Section 3. A summary is given in Section 4.

2. COMPENSATION FOR CLOCK DIFFERENCE

As shown in Figure 1, a Demod/Remod system provides transparent connection between two Modems/Fax M_1 and M_2. The four separate units involved in this connection have independent clock generators. The two ends of the relay system R_1 and R_2 may or may not share the same clock. Thus, at least three independent clocks exist in the overall connection. The ITU recommendation [3] allows a maximum of ±0.01% tolerance in the baud rate frequency. In a direct connection of two voice band modems, each modem synchronizes its receiver with the other modem transmitter clock, via a clock recovery method [4,5]. However, when a Demod/Remod relay system mediates the connection, the synchronization process is more complicated. The amount of data demodulated in one side is different from the amount modulated at the other side. Eventually, one or both sides of the relay will either starve for data or lose data due to buffer under/overflows. The transmitter in the each side of the Demod/Remod relay must tune its clock with the receiver at the other side.

The clock adjustment presented in this paper is composed of buffers in either side of the relay, use of bandwidth overhead to transmit data offset and a closed loop feedback control to tune the transmitter clock. The buffers keep track of the increase or decrease in the amount of data due to clock differences. This is discussed in more details in the following.

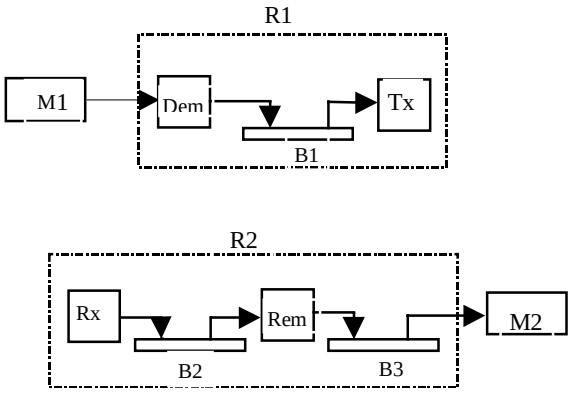

Figure 2: Demod/Remod Buffers

Figure 2 shows how First-In-First-Out (FIFO) buffers are used to store and control the data flow between the two ends of the relay system. For simplicity, a half duplex data transmission – from modem M_1 to modem M_2 is shown in this figure. The passband signal received from modem M_1 is demodulated. The demodulated data is stored in FIFO buffer B_1. Due to the clock difference between M_1 and the relay unit R_1, the amount of data buffered in each processing frame may be different from the nominal value. If the offset passes a threshold, the data transmitted through the wireless channel will be increased/decreased in one (or a few) processing frames. Two different thresholds are set for negative and positive data offset to allow a hysteresis in data count switching. This hysteresis is essential to avoid sudden reactions to temporary changes in the buffer count due to jitter, etc.

On the other side of the wireless link, the data received by the wireless receiver is buffered into FIFO buffer B_2 before being sent to the re-modulator. The number of data symbols fed from this buffer to the modulator will be incremented or decremented from the nominal value, if the data offset in buffer B_2 exceeds positive/negative thresholds. The bandwidth excess, due to transmission of additional data, is minimized by transmission of one extra data bit per processing frame (5 or 20 ms). Therefore, buffers B_1 and B_2 are also used for converting data formats from symbols to bits and bits to symbols, respectively. The extra/missing bit per frame plus its status information can be encoded in two bits as shown in Table 1. The maximum bandwidth excess due to this transmission, which occurs at data rate 4800 bps , for a V32 standard modem with 5 ms processing frames, is 8.3%.

Table 1: Dibit encoding of additional data per frame.

Status	Encoded dibit
No extra/missing bit	00
Extra bit = 1	01
Extra bit = 0	10
One missing bit	11

Finally, buffer B_3 stores the 8 kHz passband modulated samples. This buffer is essential for two reasons, first to provide a constant stream of samples for the PCM channel, regardless of the number of data symbols fed into the modulator. Secondly, the offset between the sample count in this buffer and the nominal value is used as error signal in a negative feedback loop to tune the transmitter clock as described in the next sub-section.

Transmitter Clock Adjustment

In order to avoid over/under flow of samples in buffer B_3, the transmitter clock is adjusted based on the sample count offset in B_3. This is done by tuning a parameter called clock skew in the transmitter multi-rate filter. A closed-loop control for clock skew tuning is shown in Figure 3, in which the Function H is the controller, G represents the relationship between the clock skew s and

the offset in the number of bandpass samples generated in each frame. The quantization function *Q* is due to the fact that the observation of the offset in buffer B_3 is in the form of integer numbers. Input *R* is the reference offset, $R = 0$ and *C* is the observation of the sample count offset.

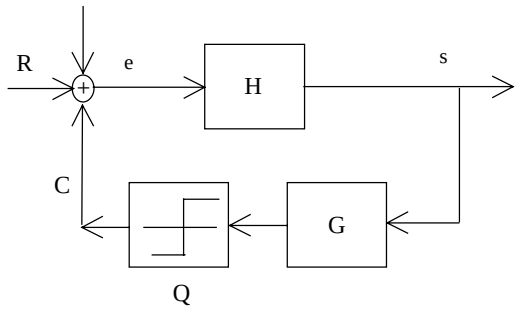

Figure 3: Control loop for clock adjustment

The clock skew adjusts the sample rate based on the following equation.

$$f_s = f_b \frac{u}{d+s}$$

where f_s is the sampling rate, f_b is the baud rate and *u* and *d* are two constants. Based on the fact that $\frac{s}{d} << 1$, the function *G* can be represented via the following linear equation.

$$G = \frac{k_1}{1 - z^{-1}}$$

where

$$k_1 = \frac{f_b u}{d^2} T$$

and *T* is the update period of the feedback loop.
A properly selected *T* (1-2 seconds) can reduce the effect of quantization noise caused by *Q*, while having a response time that maintains a reasonable size for buffer B_3.

The function *H* is designed such that the closed loop control function yields an error free steady state response to step inputs with no overshoot and a smooth transition in the clock rate.

$$H = \frac{k_2}{1 + \alpha z^{-1}}$$

Parameters k_2 and α are selected to yield a critically damp condition with a time constant of at least 5 seconds.

3. EMULATION RESULTS

Real-time tests of the VFDR relay system are performed to evaluate the performance of the clock compensation method presented in this paper. Two standard V.32 modems, from two different manufacturers, are connected via the DSPSE VFDR relay system. The impairments in one side of the relay system were emulated via a network emulator. The other side of the VFDR relay had an ideal, no impairment connection. This is true in an actual VFDR connection in which one side has an almost ideal connection with no network impairment and a very short local loop. The digital link between the two VFDR relays were also emulated ideally with no impairments.

Bit error rate (BER) vs. the PCM channel signal to noise ratio for two cases of relay with and without clock compensation are measured. The DTE and DCE are set as specified in TSB38 standard[6]. The BER curves for V.32 standard at 9600 bps are plotted in Figure 4. It is observed that in this test, in which synchronous connections exist between DTE's and DCE's, compensation for the clock difference is crucial and ignoring clock difference severely degrades the performance of the relay system. While the clock compensated relay maintains bit error rates in the order of 10^{-7}, the relay without clock compensation has unacceptable error rates in the order of 10^{-3}.

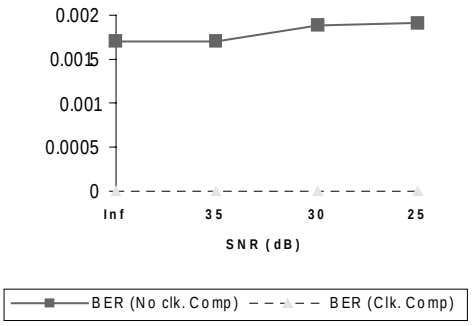

Figure 4: Bit Error Rate vs. SNR with and without clock compensation.

4. SUMMARY

A novel approach to overcome problems associated with independent clock in a data/fax relay system is presented in this paper. This approach consists of transmission of

additional data with minimum increase in the bandwidth and use of a control loop to adjust the transmitter clock in each side of the relay system. Experiments show significant progress in the performance of the relay system when this technique is used.

5. REFERENCES

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