Low Power Real-Time Programmable DSP Development Platform for Digital Hearing Aids

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ABSTRACT

This paper presents a new low power binaural wearable digital hearing aid platform based on the Texas Instruments TMS320C5000 fixed point digital signal processor. This platform is a real-time system capable of processing two input speech channels at a 32KHz sampling rate for each channel and driving a stereo headphone output. It provides for frequency shaping, noise suppression, multiband amplitude compression, and frequency dependent interaural time delay algorithms. Since the platform is a programmable solution capable of running at 1.8V for MIPS intensive research and 1V for actual hearing aid implementation, this platform will enable further research into improving the quality of life for the hearing impaired.

1. INTRODUCTION

The recent development of commercial hearing aids with digital signal processing (DSP) capabilities has allowed the development of advanced signal processing techniques to aid the hearing impaired. However, in order to meet the small size and ultra-low power requirements of hearing aids, the existing solutions have resorted to hardwired devices or proprietary architectures with minimal computational performance (MIPS). This restricts researchers from advancing significantly beyond the current algorithms due to the lack of a general purpose and fully programmable architecture with sufficient computational capability to implement complex algorithms. To overcome this limitation, this paper describes a new low power real time binaural digital hearing aid platform based on the Texas Instruments TMS320C5000 [1] fixed point digital signal processor family. It is a real time system capable of sampling up to two input speech channels at a 32KHz rate and driving a stereo headphone output. This 1.8V development platform allows researchers to use the full speed of the TMS320C5000 (currently at 100MIPS) for experimentation and development of sophisticated hearing aid algorithms. These same TMS320C5000 devices can then be used at a reduced power supply voltage of 1V and reduced number of MIPS for the final implementation in the hearing aid. This platform allows researchers to explore new algorithms while providing the portability required for laboratory as well as real world testing and final implementation.

2. SPEECH PROCESSING ALGORITHMS

Sensorineural hearing loss is characterized by a loss of sensitivity to sounds that varies with signal level and frequency response [2]. Speech enhancement can be used to separate the high and low frequencies and improve speech comprehension and listening comfort. This requires a gain adjustment that is both level-dependent (or syllabic compression) as well as multi-frequency dependent [3]. The block diagram in Figure 1 represents the speech enhancing algorithms implemented on the binaural wearable digital hearing aid platform [4]. The audiologist combines these algorithms in various configurations to provide the maximum benefit to the hearing impaired person.

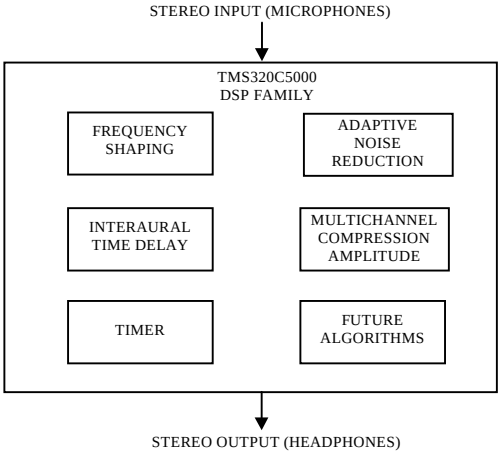

Figure 1. Speech Processing Algorithms for the Binaural Wearable Digital Hearing Aid Platform

2.1 Frequency Shaping

This platform implements a binaural equalizer using two banks of bandpass filters, one for each ear. This provides for frequency shaping from DC to 16KHz using a variable number (1 to 50, typically 14) of Finite Impulse Response (FIR) filters. Each one of these FIR filters has 50-200 taps which allows for precision frequency shaping. Linear phase is maintained across the entire frequency bandwidth, and greater than 80dB band isolation is achieved.

2.2 Adaptive Noise Reduction

The binaural wearable digital hearing aid platform also incorporates noise suppression as an integral part of the hearing aid. The algorithm works with dual (right and left ear) single input single output channels. First, the input signal is conditioned by a highpass filter to compensate for the low frequency spectral tilt in speech signals [5]. The core of the adaptive speech enhancement algorithm is the Real-Time Adaptive Correlation Enhancer (RACE) which provides active noise suppression. RACE is essentially an open-loop adaptive FIR filter. RACE estimates a short-term autocorrelation function of the input signal and uses it to update the adaptive FIR coefficients. To implement the multichannel version of RACE (MRACE), as shown in Figure 2, the bandpass filtered output of each filter is either processed through the RACE stage or delayed by the appropriate lag value [5].

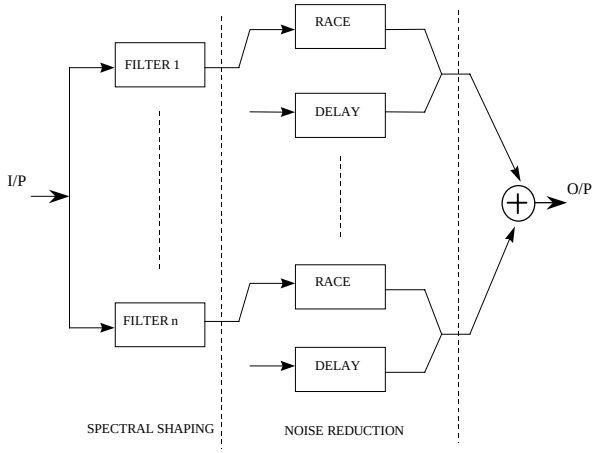

Figure 2. MRACE Block Diagram

This scheme allows the user the flexibility to enhance only those frequency bands where the noise level is predominant. The bands which do not need noise reduction are simply delayed by twice the maximum lag value in RACE before the outputs of all the filters are combined.

2.3 Amplitude Compression

In addition to frequency shaping and noise suppression, the platform also permits real time implementation of multiband amplitude compression and frequency dependent interaural time delay algorithms. Speech amplitude compression is the task of controlling the overall gain of a speech amplification system. It essentially "maps" the dynamic range of the acoustic environment to the restricted dynamic range of the hearing impaired listener. Multiband compression is achieved by applying a gain of less than one to a signal whenever its power exceeds a predetermined threshold. The time constant of power estimation is used to modify the attack/release time of the compression algorithm [6].

2.4 Interaural Delay

The importance of interaural time difference (ITD) and interaural intensity difference (IID) in speech perception and localization has been well documented [7]. This platform implements an interaural time delay algorithm that involves splitting the input signal into multiple frequency bands, interpolating the data to provide suitable time delay increments, differentially delaying the left and right inputs in each frequency band and then recombining the left and right frequency bands respectively for output to the earphone.

3. LOW POWER DSP PLATFORM

3.1 Functional Block Diagram

The functional block diagram for a programmable digital hearing aid is shown in Figure 3.

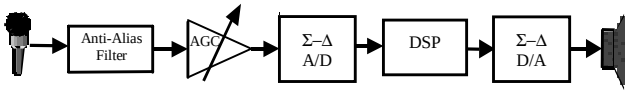

Figure 3. Functional Block Diagram

A low noise microphone converts the incoming sound into an analog signal. This signal is then processed through an anti-alias filer to remove high frequency components. A variable gain amplifier with a compression-limited input stage amplifies the signal prior to the analog-to-digital conversion stage. The analog-to-digital conversion is performed using a 16-bit sigma-delta codec to ensure sufficient dynamic range with a conversion rate of at least 16KHz to ensure adequate sampling of the speech phonemes. Ideally, a sampling rate of 32KHz would be preferred in order to provide a quality audio signal to the listener. This platform offers sampling rates up to 48KHz, but at a higher power consumption.

Once the data is converted to the digital domain, the DSP processes the digital stream using the various algorithms described in Section 2 to enhance the speech input. Non-volatile memory is used to store the audio processing algorithms, as well as the parameters for gain control, peak output, and various filter parameters. These parameters are determined through a set of tests performed by an audiologist when the hearing aid is fitted to the user.

The sigma-delta codec converts the processed digital data back to an analog waveform. This waveform is amplified and driven to the speaker. The speaker's impedance acts as a low-pass filter, removing any high-frequency quantization noise. This system must operate from a Zinc-Air battery (1.4V, 60mA-hr), which implies a total current draw on the order of 1-2mA for an operational battery life of 30-60 hours. The end-of-life battery voltage for this battery is approximately 0.9V

3.2 Low Power Binaural Platform

Figure 4 depicts the low power binaural hearing aid block diagram. This platform was implemented using a TMS320C54x with large on-chip RAM operating at 1.8V. The TMS320C54x has several power-down modes to minimize power consumption when idle. Unfortunately, the entire system cannot operate at 1.8V since currently available catalog 16-bit codecs require a 2.7V supply. Also, to drive the headphones, this application requires a stereo headphone amplifier driver that also requires a 2.7V supply. This amplifier would normally not be present in the hearing aid implementation. This prototyping system allows the researcher to explore new algorithms with high levels of computational performance (currently 100 MIPS at 1.8V) and then use the same programmable DSP architecture with optimized software for operation at 1V and the reduced MIPS rate of approximately 20-30MIPs.

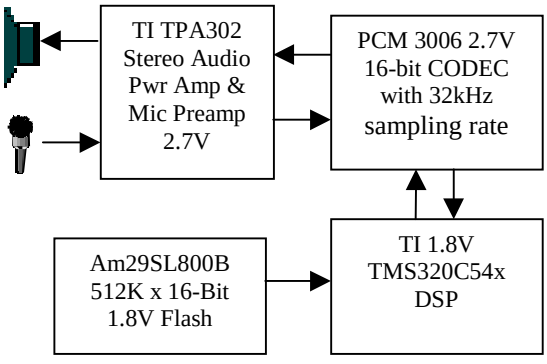

Figure 4. Low Power Binaural Hearing Platform

For the final hearing aid application, a 1V voltage regulator is required to maintain a constant power supply independent of battery voltage. A voltage doubler is also required to provide the necessary 1.8V for the codec. Eventually, both the D/A and the voltage doubler could be integrated into the digital signal processor. This approach not only saves space, which is very critical for completely-in-the-ear hearing aids, but also saves power in the final hearing aid implementation. Integrating the D/A into the digital signal processor is achieved by replacing the D/A portion of the codec with a pulse width modulated (PWM) output from the processor. This PWM signal is then amplified with a Class-D amplifier. This is the most power efficient method since The speaker impedance is used to demodulate and filter the PWM output, which results in an audio quality signal to the ear [8,9]. In the future, availability of 1V A/Ds would remove the need for a voltage doubler. The final hearing aid device would then consist of the DSP, A/D, Flash memory, and Class-D amplifier.

3.3 Power Analysis

Advances in VLSI technology are providing increasing computational performance and lower power consumption in digital signal processors that enables these devices to be used in power critical applications such as hearing aids [10]. Figure 5 summarizes this trend through the last ten year and depicts an order of magnitude decrease in power every five years. While the performance has increased from 20 MIPS to 100 MIPS, the power dissipation has decreased at an even faster rate.

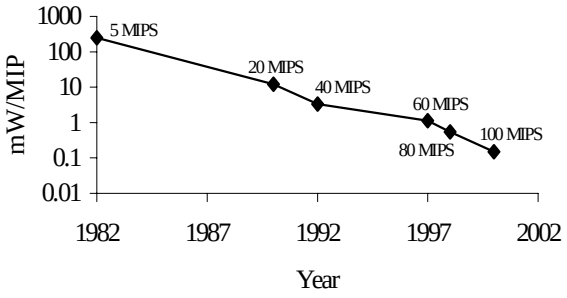

Figure 5. Power Dissipation Trends in DSP

Figure 6 illustrates the performance of the TMS320C5000 as a function of supply voltage. As the silicon geometry decreases, the TMS320C5000 low voltage operation improves. For example, the 0.18 µm process technology provides 20-30 MIPS performance at 1V while the 0.25µm process provides only 10 MIPS.

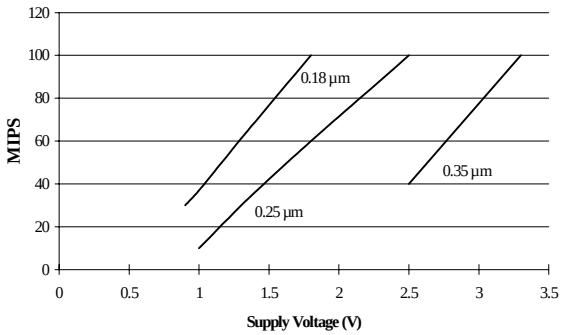

Figure 6. TMS320C5000 MIPS vs. power supply

In the last two years, power dissipation has taken a dramatic decrease as shown in Table 1. In 1998 power consumption was 0.25mA/MIPS at 1.0V (0.25mW/MIPS) and provided 10 MIPS total processing power. The 1999 version consumes only 0.18mA/MIPS at 1.0V (0.18mW/MIPS) providing about 20-30 MIPS of total processing power. This same device is available at 1.8V with 100 MIPS processing power and 0.32mA/MIPS (0.576mW/MIPS) power consumption. At this rate, processors eventually could be developed that run off body heat.

Table 1. TMS320C5000 Power Efficiency

Technology	Voltage (V)	Performance (MIPS)	Power (mA/MIPS)
0.44 µm (1996)	**3.3 V**	**50**	**0.8**
0.35µm (1997)	**3.3 V**	**66**	**0.6**
0.25 µm (1998)	**2.5 V**	**100**	**0.45**
	1.0 V	**10**	**0.25**
0.18µm (1999)	**1.8 V**	**100**	**0.32**
	1.0 V	**20-30**	**0.18**

4. CONCLUSIONS

A new low power binaural wearable digital hearing aid platform based on the Texas Instruments TMS320C5000 fixed point digital signal processor family was developed. The programmability and portability of this system provide a significant improvement over existing hardwired or proprietary solutions for several reasons. First, everyone's hearing loss is different and thus the speech enhancing algorithms need to be tuned to the particular hearing impairment. Second, a person's hearing loss might change with time thus requiring updates in their hearing aid. Third, the speech enhancement algorithms need to adapt to the environment to provide optimum hearing compensation and listening comfort. Fourth, researchers need an open programmable system that allows unbounded performance for algorithm development, yet still provides a low power solution for the final product without modifying the software. Finally, since this solution utilizes a standard catalog part, hearing aid devices can leverage the algorithms already implemented in this architecture to increase the number of features. As these low power programmable devices become available, more sophisticated algorithms and longer battery life will result in an improved quality of life for the hearing impaired.

5. REFERENCES

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