PHASE NOISE IN SAMPLING AND ITS IMPORTANCE TO WIDEBAND MULTICARRIER BASE STATION RECEIVERS

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ABSTRACT

Future base stations for the narrowband cellular standards, e.g GSM and D-AMPS, will deploy wideband multicarrier receivers. In these receivers the phase noise of the sampling stage is crucial in order to meet the blocking performance specified in the standards. In this paper an expression relating the single sideband phase noise power density to carrier ratio of a sampled signal to that of the sampling clock is derived.
The implications of the theory for the clock local oscillator (LO) and clock drive amplifier for a GSM-1900 receiver are shown.

1. INTRODUCTION

For some radio receiver applications, e.g wideband multicarrier base station receivers [1], the phase noise performance of the sampling clock is important. It is not only required that the Signal-to-Noise Ratio (SNR) in the Nyquist bandwidth due to the clock phase noise is known, but also that the spectral shape of the noise on the sampled signal can be predicted.
In this paper the basic relationships regarding phase noise in sampling will be derived and some implications for the application mentioned above will be studied.

2. PHASE NOISE IN SAMPLING

2.1 Basic Relationships

Assume that a sinusoidal signal is sampled at the time instants

$$t_n = n \times T_s + \varepsilon_n \qquad (1)$$

where T_s is the sampling period, ε_n is a random variable representing the time jitter and n is an integer.
The sampled signal then becomes

$$X_n = X(t_n) = \sqrt{2P} \times \sin(2\pi f_{in}(n \times T_s + \varepsilon_n) + \phi_0) \qquad (2)$$

Where P is the average power in the signal and ϕ_0 is an arbitrary phase angle.
The analysis of the effects on the sampled signal by the noise of the sampling clock can be much simplified by using a sinusoidal representation for narrowband noise and thereby be able to use modulation theory instead of having to get involved in rather complicated calculations based on the statistics of the random variable ε_n.
For this purpose, let the clock have 1 Hz phase noise sidebands at frequency offsets +/- f_m with a single sided (phase) noise power in 1 Hz of N_{phase}, as illustrated in figure 1.
If the power in the clock carrier, C, is much larger than the sideband noise power (i.e the peak phase deviation is small), the phase noise sidebands can be considered to originate from phase modulating the clock carrier with

$$\varphi(t) = \sqrt{\frac{4N_{phase}}{C}} \times \sin(2\pi f_m t) = \varphi_{peak} \times \sin(2\pi f_m t) \qquad (3)$$

$$= 2\sqrt{L(f_m)} \times \sin(2\pi f_m t)$$

Where $L(f_m) = N_{phase}/C$ is the single sided noise power density to carrier ratio of the clock.
The above statement relating $L(f_m)$ and the phase deviation of the clock is fundamental to the derivation that follows and it is straightforward to verify that the relation is true by expanding the modulated signal in Bessel functions and further simplify by using the assumption of the small peak phase deviation.

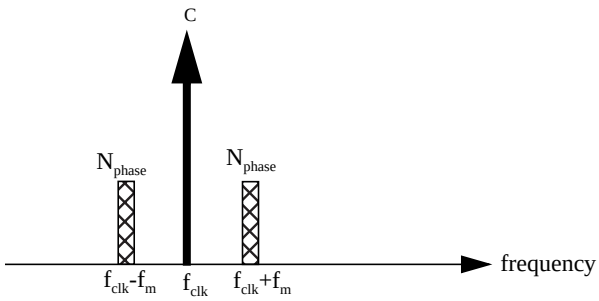

Figure 1. Clock signal with phase noise sidebands. Levels are average power.

The error in phase between the actual and ideal sampling clock is changed with a rate of f_m and with a peak deviation of φ_{peak}.

In the time domain this means that the equivalent time error, i.e deviation from the ideal sampling instants, will also vary with a rate of f_m and with a peak time deviation of

$$T_{peak} = \frac{\varphi_{peak}}{2\pi f_{clk}} \quad (4)$$

The time jitter hence becomes

$$\varepsilon_n = T_{peak} \times \sin(2\pi f_m n T_s) = \frac{\varphi_{peak}}{2\pi f_{clk}} \times \sin(2\pi f_m n T_s) \quad (5)$$

and the sampled signal (with $\phi_0 = 0$)

$$X_n = \sqrt{2P} \times \sin\left(2\pi f_{in} n T_s + \varphi_{peak} \times \frac{f_{in}}{f_{clk}} \times \sin(2\pi f_m n T_s)\right) \quad (6)$$

Equation 6 states that the sampled signal will be phase modulated with a frequency of f_m and a peak phase deviation (or modulation index) that is the same as that of the clock signal multiplied by the ratio of the input and clock signal frequencies.
It is again straightforward to verify that the implication of this is that the sampled signal will have noise sidebands at the same off-set frequencies as the clock signal, but the relative amplitude of these will be multiplied by the ratio of the signal frequency to the sampling frequency. This is illustrated in figure 2. As before, this is only valid if the peak phase deviation is small.

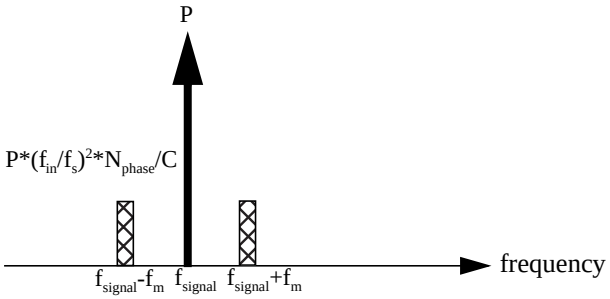

Figure 2. Noise sidebands of the sampled signal. Levels are average power.

In figure 3 the effect of sampling with a clock that has sidebands from phase modulation can be seen. The simulations are performed with two different ratios of input and sampling frequencies. The sidebands should in theory differ by 20 X $\log_{10}$(6.25/0.25) = 28 dB and both be offset with 0.1 X f_s from the signal itself, which is exactly what can be seen from the spectrum plots.

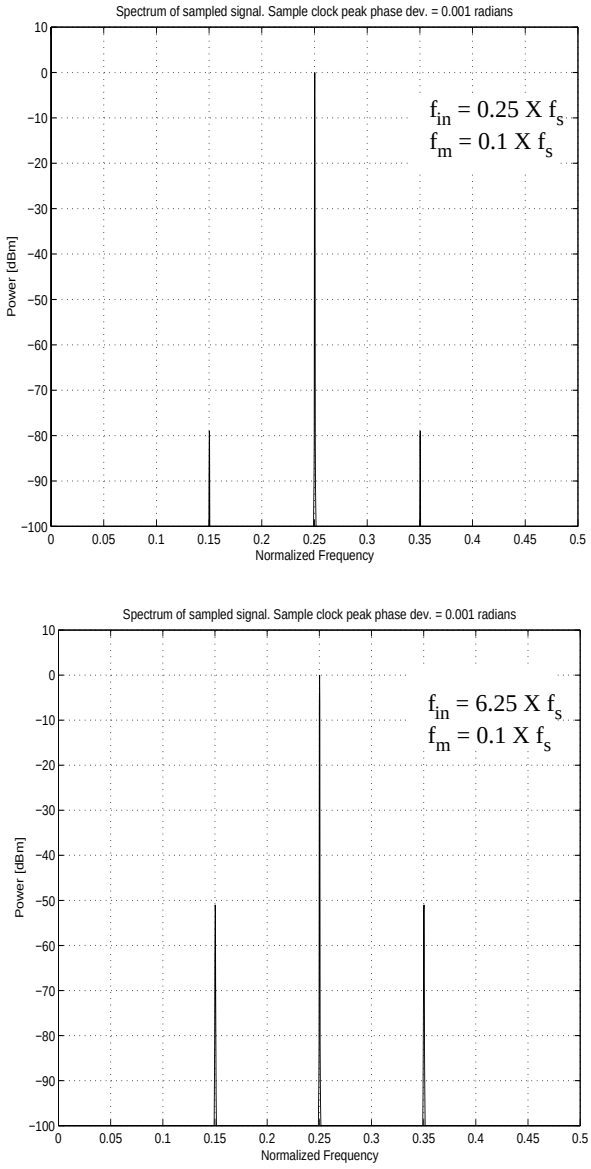

Figure 3. Spectra of sampled signals when the sampling clock has 'noise' sidebands originating from phase modulation at a rate of 0.1 x fs

2.2 Clock Limited Signal-to-Noise Ratio

From equation 6 the peak phase deviation of the sampled signal is

$$\varphi_{signal} = \varphi_{clock} \times \frac{f_{in}}{f_{clk}} \quad (7)$$

Where φ_{clock} is the peak phase deviation of the clock.
It has already been stated that the peak phase deviation is related to the single sideband noise power density to carrier ratio, $L(f)$, by

$$\varphi_{peak} = 2\sqrt{L(f)} \quad (8)$$

After squaring, equation 7 then becomes

$$L_{signal}(f_m) = L_{clock}(f_m) \times \left(\frac{f_{in}}{f_{clk}}\right)^2 \quad (9)$$

Now, integrating equation 9 over offset frequency leads to

$$SNR_{signal} = \left(\frac{f_{clk}}{f_{in}}\right)^2 \times SNR_{clk} \quad (10)$$

Equation 10 gives the actual measured SNR for the sampled signal only if the dominant source of noise is the sampling clock phase jitter. In other cases, e.g when contribution from thermal or quantization noise is significant, the formula only indicates how much of the total noise that is contributed by clock phase noise.
Note that equations 4 and 6 imply that

$$\varphi_{signal} = 2\pi f_{in} T_{peak} = 2\sqrt{L_{signal}(f_m)} \quad (11)$$

so that

$$L_{signal}(f_m) = \left(2\pi f_{in} \times \frac{T_{peak}}{2}\right)^2 = \left(2\pi f_{in} \times \frac{t_{fm}}{\sqrt{2}}\right)^2 \quad (12)$$

Where t_{fm} is the rms value of the time jitter originating from phase noise in a 1 Hertz bandwidth at frequency offset f_m, i.e it is the rms time jitter spectral density. Integrating equation 12 over frequency then gives

$$SNR_{signal} = \frac{1}{(2\pi f_{in} t_a)^2} \quad (13)$$

Where t_a is the rms time jitter.
Equation 13 is the expression for the clock limited SNR often found in literature [2] treating sampling with a noisy (jittered) sampling clock.
It is obvious that equations 10 and 13 express the same thing, even though the rms time jitter (aperture jitter or uncertainty) is implicit in the former.
For receiver applications the most convenient expression is given by equation 9 since normally the required phase noise performance of the sampled signal is given as a function of offset frequency and then the clock phase noise requirement can easily be determined.

3. Implications for Multicarrier Receivers

It is reasonable to believe that coming generations of base stations for the cellular systems of today, e.g GSM and D-AMPS, will incorporate wideband multicarrier receivers in order to reduce cost and size and also to allow for implementation of software defined radio [3,4]. The enabling technology for these receivers are the wideband, high dynamic range Analog-to-Digital Converters (ADCs) that are becoming available.

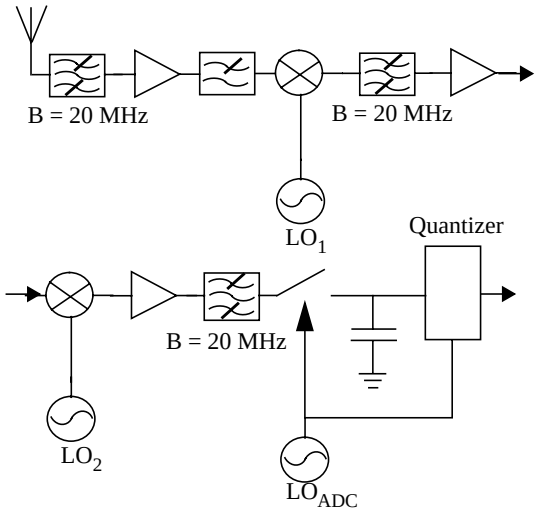

Figure 4. Analog part of a double conversion wideband receiver

In a multicarrier receiver the whole band of interest, e.g 20 MHz, is frequency translated to a final IF and sampled with a wideband, high dynamic range ADC, as illustrated in figure 4. Downconversion to baseband and channel selection is performed in the digital domain and hence there is no selectivity in the analog path that will protect the receiver IF-circuitry and ADC from being subjected to large inband interfering signals. This is a fundamental difference compared to a narrowband receiver in which only the front-end, i.e the Low Noise Amplifier (LNA) and first mixer, need to handle large interfering signals.
In a signal situation with one large blocking signal (mobile close to base) and a small desired signal (mobile far from base), the phase noise contribution to the total noise power in the channel will not only come from the first LO, but also from the second and ADC LOs. The overall requirement on phase noise must, for the double conversion receiver here illustrated, be divided between all three oscillators. For frequency offsets, f, where an oscillators phase noise power density to carrier ratio, $L(f)$, falls as $1/f^2$, [5]

$$L(f) \propto \frac{f_{LO}^2}{Q^2 \times f^2} \quad (14)$$

It may then be argued that the contribution from the second and ADC LOs can be made insignificant in this region due to the low frequencies (f_{LO}) and high Q-values (Q) that can be achieved with for instance crystal resonators.
At larger offset frequencies the noise floor will however ultimately be limited by the thermal noise of the oscillator and buffer amplifiers and reach a constant level. This means that $L(f)$, at larger frequency offsets, will become dependent on the output power of the oscillator.
As an example consider the sampling arrangement in figure 5.
To meet the GSM-1900 blocking requirement, $L(f)$ of the sampled (blocking) signal must be in the range of -140 dBc/Hz at a frequency offset of 800 kHz or more.
As already mentioned the requirement on the ADC LO is dependent on the performance of the other two LOs and it is reasonable to assume that the RF LO must be allowed to give the largest con-

tribution. Therefore the ADC LO must have a phase noise significantly lower than -140 dBc/Hz at these frequency offsets.

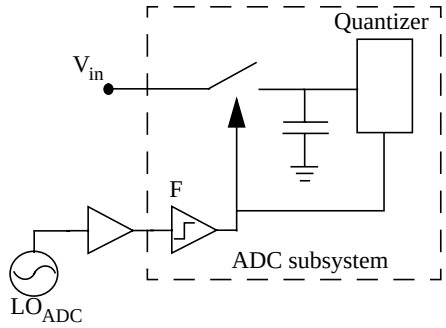

Figure 5. Receiver sampling stage.

Under the assumptions that the clock power level at the input of the ADC subsystem is 0 dBm and that only phase noise (and not amplitude noise) from the clock driver is significant, the requirements on its noise figure can be calculated as a function of the LO_{ADC} L(f) referred to the input of the ADC subsystem. This has been plotted in figure 6 for requirements of -145 dBc/Hz and -150 dBc/Hz. The sampling frequency is 60 MHz and the signal band of interest is either 5 to 25 MHz or 65 to 85 MHz, i.e the signal will be in the first or third Nyquist bands, respectively.

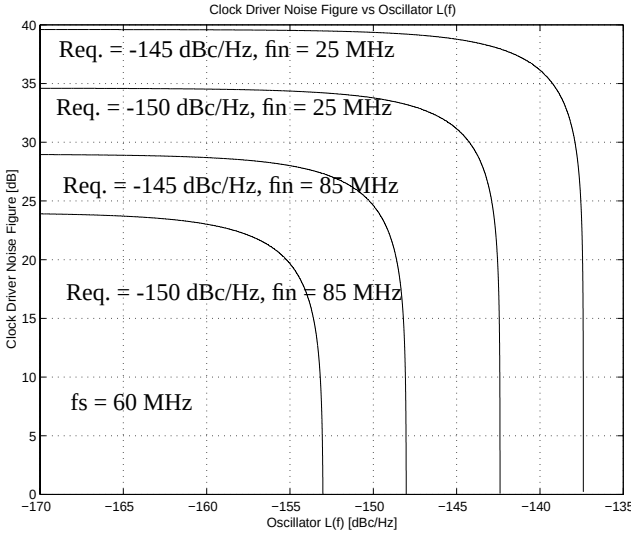

Figure 6. Required combination of LO phase noise and clock drive amplifier noise figure.

From the plot it can be seen that the requirements on the ADC clock driver noise figure is low to moderate, but it is obvious that when designing the on-chip clock driver circuitry for an ADC intended for multicarrier base station applications, the noise performance must be a design parameter.
It can also be seen that undersampling the signal at a high IF in order to save one stage of downconversion or simplify receiver frequency planning puts large requirements on the ADC LO noise floor, but imposes no unrealistic requirements on the ADC clock driver noise figure.

4. SUMMARY

The effect on a sampled signal by the phase noise of the sampling clock has been studied. It has been shown that noise sidebands of the sampling clock is transformed to noise sidebands of the sampled signal at the same frequency offsets, but with amplitudes which are those of the clock sidebands multiplied by the ratio of the signal frequency to sampling frequency.
As a special case of phase noise in sampling a multicarrier receiver for a base station application was studied. It was shown that even though the close-in phase noise may not be a problem, the noise floor at larger frequency offsets may limit the blocking performance of the receiver. The requirements on the clock driver noise figure for a Nyquist-sampling receiver are however not very severe and even for moderate undersampling ratios the requirements are not unrealistic.

5. REFERENCES

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