MULTIMEDIA APPLICATIONS OF MICROPROCESSOR WITH EMBEDDED DRAM

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ABSTRACT

The M32R/D is a 32-bit microprocessor with large-capacity on-chip DRAM. It consists of a 32-bit RISC CPU, a 32-bit x 16-bit multiply and accumulator (MAC), either 1-Mbyte or 2-Mbyte DRAM, 4-Kbyte cache memory, and a memory controller. The CPU, DRAM, and cache memory are connected via a 128-bit 66.6 MHz internal bus yielding high performance and low power dissipation. The chip is capable of coping with a wide range of applications and thus provides system designer with great flexibility. For instance, a portable multimedia system can be realized by only three chips: an M32R/D chip, an I/O ASIC chip, and programming ROM. This means that a total system solution can be achieved at a lower cost with higher performance. Personal digital assistants (PDAs) and digital still cameras are such examples.

1 . INTRODUCTION

Portable multimedia systems, such as personal digital assistants (PDAs), intelligent cellular phones, digital cameras, and car navigation systems, etc., are newly emerging. Design of these application systems calls for lower power consumption while maintaining reasonably high performance. However, until now, implementation solutions have only been partially successful. This is because there have been few processors that satisfy the requirements of portable multimedia systems. Designers of microprocessors for desktop computers have focused on high speed rather than low power dissipation and microcontroller designers have taken low power dissipation as a first priority. Because of this, dedicated hardware modules have been needed to complement the performance of microcontrollers with low cost, low power, and low performance. Unfortunately, these dedicated hardware modules are of little use in different applications due to the inherent inflexibility in their design and thus make the system cost high.

There are several approaches to reducing power dissipation while keeping high performance. Utilizing advanced process technology is one of them. Another approach is merging DRAM with a high performance RISC processor on a single silicon chip. A 32-bit RISC microprocessor with large-capacity embedded DRAM—M32R/D—is an implementation of the latter approach [1]. The main advantage of merging a microprocessor and DRAM is feasibility of using a wide and fast internal bus. Since the transactions of the external bus can be reduced with this configuration, it is possible to make the external bus narrow and slow. With a 128-bit 66.6MHz internal bus and a 16-bit 16.6MHz external bus, the M32R/D achieves high performance and low power dissipation with low cost [2].

This paper highlights a couple of examples of system solutions utilizing M32R/D's unique DRAM integration. This paper is organized as follows. In Section 2 we introduce the architecture of the M32R/D. In Section 3 we then discuss the architectural advantage of the M32R/D. In Section 4 we show application systems that utilize the M32R/D's high performance and low power advantages.

2 . ARCHITECTURE

The M32R/D incorporates a CPU with large-capacity DRAM on one chip. Figure 1 shows the block diagram of the M32R/D. The chip consists of:

- a small RISC CPU core, with a simple instruction set of 83 instructions;
- a 32-bit x 16-bit multiply accumulator (MAC);
- 1 Mbyte or 2Mbyte DRAM;
- a 4K-byte cache, which is direct mapped with 128-bit block size and follows a write-back policy; and
- an external bus interface unit (BIU).

The CPU, DRAM, cache, and BIU are connected with a 128-bit 66.6MHz internal bus. The internal bus is connected to a 16-bit 16.6MHz external bus through the BIU.

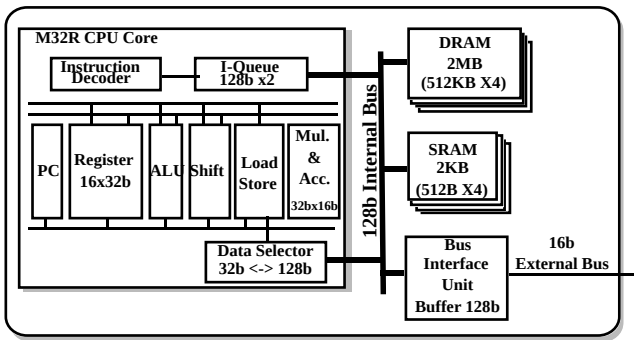

Figure 1. Block diagram of M32R/D.

As illustrated in Figure 1, the M32R/D has two 128-bit entries of the instruction queue (I-Queue), a 32<-->128 data selector for operand reads/writes by the CPU, and a BIU buffers. The

BIU buffer is a 128-bit data buffer and supports burst transfers on 128-bit bounded data. This is effective for high speed data transfers from the external ROM to the cache and from the DRAM to the outside.

The 128-bit internal bus operates at 66.6MHz and transfers 128 bits of data between the CPU and memory in one cycle. The number of access cycles of memory is as follows:

- On a cache hit, the number of access cycles is 1 (i.e., no wait cycle). In an operand access, 32 bits of data is transferred between the CPU and the cache in one cycle through the 32<-->128 selector. In instruction fetch operations, 128 bits of instruction code are fetched into the I-queue in one cycle. In this way the CPU is able to get 4-8 instructions in one cycle.
- On a cache read miss, the data transfer from the DRAM to the CPU and the update of the cache data takes 4 cycles on a DRAM page hit or 8 cycles on a DRAM page miss.
- On a cache write miss, the data transfer between the cache and the CPU takes only 2 cycles (i.e., one wait cycle). This is because the cache has a write buffer for the CPU so that the CPU does not need to wait for the data transfer from the cache to the DRAM to be completed.

3. ARCHITECTURAL ADVANTAGES

A comparison of application system configuration between a conventional system configuration and M32R/D is shown in Figure 2. In a conventional system, a CPU and versatile peripheral circuits are integrated on the same chip and memory chips are connected via an inter-chip bus which is typically 16-bits or 32-bits wide. With this configuration, the following problems are addressed:

- Because peripheral circuits are unique to each application system, a wide range of functional combinations may be required. This makes the system design inflexible and thus makes the system cost high.
- Although high bandwidth between the CPU and memory can be obtained by wide bus width and high frequency, these factors increase the number and signal transition frequency of I/O pins and bus lines. Thus, high bandwidth results in an increase of power consumption and system cost.

In the M32R/D system, the CPU incorporates a main memory instead of peripheral circuits, and it is connected with a 128-bit internal bus. This configuration has the following advantages:

- Since the CPU and DRAM have the general purpose, the chip can be used for many application systems;
- The 128-bit 66.6MHz internal bus yields high performance while maintaining low power dissipation; and
- The external bus connected to peripheral circuits and ROM chips can be slow and narrow, which keeps power dissipation low.

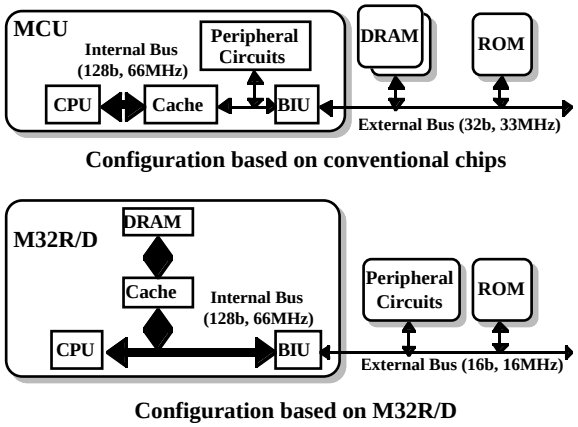

Figure 2. Application system configuration.

3.1 Performance

To test the performance of the M32R/D, we evaluated the performance of the conventional system compared to a system using the M32R/D and several application programs. Figure 3 shows the comparative execution time performance. The M32R/D system achieves higher performance in every application program, and it reaches 1.3 to 1.6 times the performance of the conventional system. The performance advantage of the M32R/D is a result of the high bandwidth (1G-byte/sec) of the internal bus. For instance, a penalty of cache miss is reduced to only 3 or 7 cycles, depending on a DRAM page hit or miss, against 16 cycles in conventional system; therefore the M32R/D continually achieves high performance despite a low cache-hit rate.

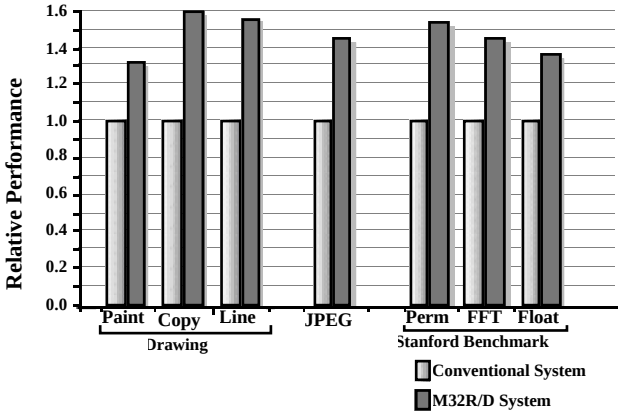

Figure 3. Comparison of M32R/D performance versus conventional systems.

3.2 Power Dissipation

A comparison of power consumption is shown in Figure 4. The power consumption of the system using M32R/D is

reduced to almost one third of that of the conventional system. This is because:

- Due to the integration of CPU and main memory, M32R/D can realize sharp reduction in the power consumption of I/O buffers driven during DRAM access;
- The DRAM's power consumption per access is lower because it does not need to drive a heavily loaded external bus; and
- The wide internal bus reduces the number of DRAM reads and writes.

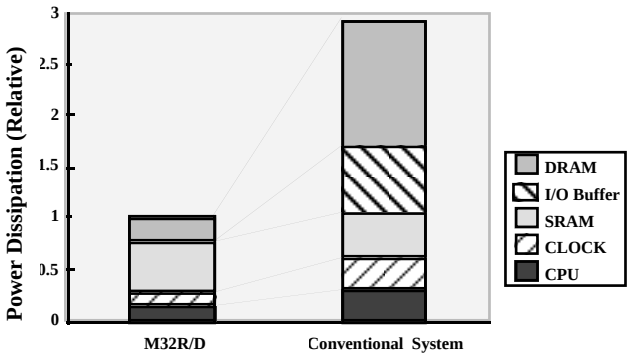

Figure 4. Comparison of power dissipation.

A battery operable portable multimedia system requires lower power consumption both during normal operation as well as on stand-by condition. The M32R/D is highly suitable for such an application system.

4. APPLICATION SYSTEMS

4.1 On-chip DRAM for Unified Memory Architecture

In recent systems that have a graphical user interface (GUI) and unified memory architecture (UMA), the main memory is shared by frame memory for display data. In the conventional system as shown in Figure 2, performance will be degraded because of bus conflicts resulting from periodic data transfer from main memory to the display device. This situation is caused by transferring only 32 bits of data at a time. In a system employing the M32R/D, the 128-bit wide bus range between the DRAM and the BIU is very efficient in avoiding this effect. That is, the 128-bit display data is transferred from DRAM to BIU first, and then the display data are transferred from the BIU to the external display in 16-bit units while the CPU core makes concurrent access to DRAM. Therefore, only 12 cycles (3-1-1-1-1-1-1-1 and 2 arbitration) are required to read data from the on-chip DRAM by the external bus masters.

Table 1 shows the bus occupancy ratio based on the frequency used to transfer data to the display. We assumed that the resolution and the number of bits per pixel for each application are as listed in the table. The internal bus occupancy ratio for all application systems is less than 10 percent. As for the external bus, bus traffic for the display is reduced to approximately 10 percent with a PDA using an LCD (320 by 240, 4 bits per pixel). Even in car navigation and set-top box systems, the external bus occupancy ratio is only increased to 40 percent.

Taking advantage of the M32R/D's integrated 2Mbyte DRAM allows the UMA to be easily constructed and product cost to be reduced.

Table 1. Bus occupancy ratio for display

Application system	Resolution, bits/pixel	Frame buffer size (byte)	Dot clock (MHz)	Bus occupancy ratio (%)
PDA	320x240, 4	37.5K	5	11 (external) 1 (internal)
set-top box	640x480, 8	300K	14.3	42 (external) 5 (internal)
car navigation	320x240, 4	37.5K 4 planes	7.15	48 (external) 6 (internal)

4.2 Examples Of Application Systems

As stated earlier, the M32R/D is designed to simplify the development of multimedia products. A system design example for a PDA is illustrated in Figure 5.

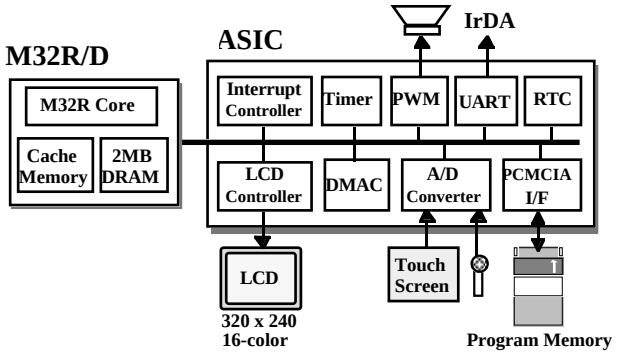

Figure 5. Block diagram of PDA.

In this example, features of a PDA to control the LCD, touch screen, and sound control are implemented as an I/O ASIC chip. Included is an LCD controller, two 10-bit AD converters for the touch screen and microphone respectively, and a pulse wave modulator for sound and UART controlling IrDA (Infrared Data Association) data communication chip. By employing the M32R/D with integrated DRAM, a PDA can be configured with only three chips: the M32R/D, a peripheral I/O ASIC (application specific IC), and program memory. This makes the entire system smaller and achieves a total system solution at a lower cost.

Another good example of the M32R/D based multimedia systems is digital still cameras. Since JPEG compression of digital image data can be done by a software library running on the M32R/D in high speed [3], it is possible to eliminate a hardware module dedicated to the JPEG compression. For example, JPEG decoding of VGA size image data (640x480 pixels) can be realized in less than 0.5 sec by the library. The M32R/D's DRAM integration yielding high performance and low power dissipation gives the great flexibility to system designers.

5. SUMMARY

The M32R/D integrates a CPU and large-capacity DRAM on one chip. It implements a 128-bit 66.6MHz internal bus connecting the CPU, on-chip DRAM, and on-chip cache. This allowed us to use a narrow and slow external bus, which results in low power dissipation and low cost while keeping the system performance high. By using the M32R/D, a multimedia system can be realized with only three chips. This results in a lower system cost and gives great flexibility to system design.

6. REFERENCES

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