STABLE ONE-BIT DELTA-SIGMA MODULATORS BASED ON SWITCHING CONTROL

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ABSTRACT

We present a globally stable arbitrary-order single-bit delta-sigma modulator architecture with continuous-time loop filtering. Using Lyapunov arguments and the method of equivalent control, it is shown that stability is guaranteed for any input signal with peak magnitude less than L > 0, where -L and +L denote the quantization levels. The design augments the conventional deltasigma modulator with switching feedback and the use of distinct operating modes: the additional circuitry required for the implementation of these stabilizing measures is nominal. For a given noise transfer function and fixed oversampling ratio, the new architecture achieves the same peak signal-to-noise-plus-distortion ratio as a traditional delta-sigma modulator. The proposed design can also yield near-peak performance for inputs which destabilize the conventional delta-sigma data converter. Simulation results are provided for the proposed modulator and a comparable standard interpolative design.

1. INTRODUCTION

Delta-sigma modulators are processing elements which use feedback and oversampling to yield low-cost, high-resolution digitization of analog signals [8]. A conventional design is shown in Figure 1. Although the quantizer, $Q(\cdot)$,¹ is single-bit, the spectral resolution of the digital output can be up to twenty bits at practical sampling rates, $\frac{1}{T_{e}}$ [7].

Despite extensive use in commercial applications, the stability of high-performance delta-sigma modulators cannot be guaranteed or characterized except in special cases. Rigorous analysis methods for converters based on aggressive noise transfer functions only exist for loop filter orders of up to three [10] [1]. While a more general stability test is available, it is often too conservative to be of practical value [2]. To mitigate the effects of instability, designers incorporate integrator reset or state-variable limiting tactics [3] which, although temporarily effective, can significantly degrade performance. Multi-bit oversampled converters are more

$$Q[\sigma(t)] := L \operatorname{sgn} \left\{ \sigma \left[\left\lfloor \frac{t}{T_s} \right\rfloor T_s \right] \right\}, L > 0,$$

$$\operatorname{sgn}(a) := \left\{ \begin{array}{c} +1, a \ge 0\\ -1, a < 0 \end{array} \right.$$

in which $\lfloor a \rfloor$ denotes the greatest integer less than $a \in \mathbb{R}$.



Figure 1: Conventional delta-sigma modulator. T_s denotes the sampling interval, e and σ represent the scalar loop filter input and output.

robust² than conventional single-bit modulators, but imperfections in the feedback digital-to-analog converter often require expensive supplemental circuitry to improve integral linearity [5] [4].

In this paper, we describe a novel single-bit modulator which achieves the same peak performance as conventional designs based on the same noise transfer function. Stability is shown rigorously through the methods of nonlinear control [9]. To prevent quantizer overload,³ the loop filter state is smoothly *driven* towards the origin using appropriate feedback. The use of two-level quantization ensures that converter linearity is preserved and helps minimize circuit complexity.

2. DESCRIPTION OF NEW ARCHITECTURE

A modulator is stable if, given a finite bound on the input signal, all loop filter states are bounded such that quantizer overload cannot occur. It is *globally* stable if it is stable for any initial loop filter state within a suitably defined set containing the origin.⁴ The proposed design is globally stable; a condensed version of the proof is given in the Appendix. Stability is ensured through the use of adaptation on the loop filter, H, according to specific rules based on the signs of the elements of the loop filter state, $x \in \mathbb{R}^n$, and quantizer input signal, $\sigma \in \mathbb{R}$. Adaptation refers to the use of memoryless, switching feedback; each integrator within the loop filter has an associated feedback gain which can switch between a finite number of discrete values. A block diagram outlining the

 $^{^1\}text{We}$ use the following quantizer and $\text{sgn}(\cdot)$ definitions throughout the paper:

²Strictly speaking, the use of multilevel quantization does not *guarantee* stability, however.

 $^{{}^{3}}Quantizer overload$ occurs if the input to the quantizer is outside the quantization levels.

⁴The set is defined as $\Omega_1 = \{x \in \mathbb{R}^n : |\sigma| < \rho\}$ in which ρ is less than or equal to the magnitude of the quantization levels. $x \in \mathbb{R}^n$ is the loop filter state, and σ is the quantizer input, as in Figure 2.

design is shown in Figure 2. A more detailed "practical version" of the design is shown in Figure 3. The topology of the adaptive loop filter, H, is shown in Figure 4, with the adjustable feedback gains, k_i , given by Equation (9). The net effect of tuning H is the generation of a stabilizing state feedback signal entering the summing junction along with r and δy of the form $K(x, \sigma)x$, in which K is a $1 \times n$ matrix whose entries depend on the signs of σ and the elements of x and rough estimates of the magnitudes of these variables (for which the coarse analog-to-digital converter (ADC) in Figure 3 is used).

In the practical version of the design, the mode selection circuitry is preceded by an analog multiplexor which feeds a coarse (three- or four-bit) ADC, for which a simple *successive approximation* or *algorithmic* design should suffice [8, Chapter 13]. The converter and memory are required to roughly estimate the size of σ and state magnitude in order to determine the appropriate switching mode.



Figure 2: Proposed (idealized) stable delta-sigma modulator architecture. Bold lines indicate buses. x denotes the loop filter state vector and sgn(·) the element-wise sign function. *Mode Selection* and *Switching* Logic are given by Equations (7)-(9).



Figure 3: Hardware-implementable version of proposed modulator architecture. A multiplexor is used to replace the comparator bank implied by Figure 2 with a single comparator. A clock signal at a fraction, 0 < m < 1, of the sampling period may be required to ensure robust operation.

2.1. Operation

The modulator has three distinct operating modes: "no-switching," "mild-switching," and "hard-switching." Each switching mode corresponds to the size of the state vector and output of the loop filter. In some neighbourhood about x = 0, all feedback gains k_i



Figure 4: Loop filter topology (all nominal poles of H are at dc in this case). Σ_0 represents the $1 \times n$ output matrix of the loop filter state-space model. The k_i feedbacks are switchable gains; explicit formulas are given in Equation (9). The x_i states denote elements of the vector x. Switching is based on the *signs*, and not magnitudes, of σ and the elements of x.

are set to zero, thus the system reduces to a conventional modulator. Further from the origin, within a user-selected region,⁵ hardswitching is used. This mode guarantees that the loop filter state returns to the origin along a trajectory which ensures that $|\sigma|$ (the magnitude of the input to the quantizer) is monotonically decreasing. Mild-switching is hard-switching with $K(x, \sigma)$ scaled-down in magnitude (and often close to zero). This mode empirically improves the robustness of the scheme without degrading performance.

3. SIMULATIONS

We compare the proposed delta-sigma modulator with a conventional single-bit design using the standard criteria of resolution and robustness with respect to a sinusoidal input signal of varying amplitude at a frequency of $\frac{F_B}{2}$. F_B represents the edge of the signal band determined by the sampling frequency, $F_s = 1$ Hz, and an oversampling ratio of 128. Throughout this section, $F_B = \frac{1}{256}$ Hz. Performance is measured in terms of signal-to-noise-plus-distortion ratio (S(N+D)R) in units of dB. FFTs of up to 16384 points are used to obtain the spectra.

Both modulator types are based on the same noise transfer function (NTF); thus the loop filter of the conventional modulator is identical to the *nominal* loop filter of the new architecture. In these studies, $|\delta| = 1$, so that the expected stable input range for the new modulator is the set of all input amplitudes on the open interval (-1, 1).

Butterworth discrete-time noise transfer functions of at least fourth-order are designed according to the "Cookbook Design Procedure" in [1, Section 4.4]. These filters are mapped to continuous-time using a transformation based on zero-order hold. All simulations are written in C and driven by a fourth-order Runge-Kutta numerical integration algorithm.

Fourth- and fifth-order Butterworth noise transfer functions are used with maximum gains of 1.56 and 1.70, respectively. The corresponding nominal loop filters are

$$H_{1_0}(s) = \frac{0.776s^3 + 0.338s^2 + 0.0890s + 0.0119}{s^4}$$
(1)

and

$$H_{2_0}(s) = \frac{0.845s^4 + 0.409s^3 + 0.127s^2 + 0.025s + 0.0024}{s^5}.$$
(2)

⁵A detailed definition of this set is given in the proof. The region can be defined so that as long as the loop filter state is within it, quantizer overload does not occur.

Table 1: Summary of Performance with Fourth-Order NTF

Input Signal Amplitude	S(N+D)R of Standard Modulator	S(N+D)R of Proposed Modulator
0.9	unstable	30.6 dB
0.6	unstable	33.3 dB
0.56	unstable	90.4 dB
0.55	unstable	91.5 dB
0.54	92.3 dB	91.2 dB
0.3	86.8 dB	84.3 dB
0.1	74.0 dB	75.1 dB

Table 2: Summary of Performance with Fifth-Order NTF

Input Signal Amplitude	S(N+D)R of Standard Modulator	S(N+D)R of Proposed Modulator
0.4	unstable	29.6 dB
0.37	unstable	45.8 dB
0.36	86.2 dB	85.8 dB
0.3525	unstable	84.2 dB
0.35	87.9 dB	87.6 dB
0.25	85.6 dB	83.1 dB

Outcomes for each loop filter are shown in Tables 1 and 2. The results confirm that the new architecture is more robust than the conventional. Resolutions of up to 15 bits are obtained in cases where the conventional modulator fails to function. Simulations show that, as predicted by theory, the new modulator operates over the entire input amplitude range of [0, 1), whereas the stable operating range of the conventional design cannot be determined a priori. A representative peak performance plot for the new architecture is shown in Figure 5. Peak performance in the new architecture can be obtained even if the conventional modulator is unstable. Frequent hard-switching in the new scheme reduces the S(N+D)R since "switching noise" enters the signal band.

4. APPENDIX - STABILITY PROOF

Theorem 1 (Stability of Proposed Modulator) Consider the idealized modulator system (Figure 2)⁶ with loop filter H shown as in Figure 4 in which

- t denotes time, with initial time t = 0,
- T_s is the sampling period,
- r, e, σ and y are real scalar signals,
- $x \in \mathbb{R}^n$ is the loop filter state,



Figure 5: Peak resolution plot for new architecture (fifth-order loop filter). S(N+D)R = 87.6 dB.

- Σ_0 is the output matrix, $\Sigma_0 \in \mathbb{R}^{1 \times n}$, with elements s_i ,
- k_i are real scalar gains,
- and δ is the quantizer feedback gain.

H has the nominal model

$$H_0: \quad \begin{array}{l} \dot{x} = A_0 x + B_0 e \\ \sigma = \Sigma_0 x \end{array} \tag{3}$$

in which A_0 and B_0 are given by

$$A_{0} = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & 0 \\ 0 & 0 & \cdots & 0 & 1 \\ 0 & 0 & \cdots & 0 & 0 \end{bmatrix},$$
(4)

and

$$B_0 = \begin{bmatrix} 0 & 0 & 0 & \dots & 0 & 1 \end{bmatrix}^T.$$
(5)

We make the following assumptions:

1. The input signal, r, is bounded. More precisely, r has the following property:

$$|r|_{\infty} := \sup_{t \ge 0} |r(t)| = M_r \in \mathbb{R}, \ 0 \le M_r < \infty.$$
 (6)

- 2. H_0 is minimum phase.
- 3. $s_i \neq 0$ for all $i = 2, ..., n, s_n > 0$.

We have the following result. Let ρ be any real number such that We have the following result. Let ρ be any real number over $0 \le \rho < \infty$. Let $\Omega_1 := \{x \in \mathbb{R}^n : |\sigma| < \rho\}$ define our "no-overload" region. Let $\Omega_2 := \{x \in \mathbb{R}^n : |x_i| \le b_i\}$ be a "hyper-rectangle" contained within Ω_1 , i.e., $0 < b_i < \frac{\rho}{\sqrt{s_1^2 + s_2^2 + \cdots + s_n^2}}$,

 $i=1,\ldots,n$. Suppose the mode selection logic is chosen such that

$$mode = \begin{cases} "Hard-Switching", x \in \Omega_1 - \Omega_2 \\ "Mild-" or "No-Switching", otherwise \end{cases}$$
(7)

⁶Please note that during the hard-switching mode, for convenience we model the latched quantizer in Figure 2 as a $sgn(\cdot)$ nonlinearity. As long as T_s is sufficiently small, the stability arguments here are still valid [11].

and

$$\delta = -M_r - c_\delta, \ c_\delta > 0, \tag{8}$$

with switching logic chosen as follows:

$$k_{1} = 0$$

$$k_{i} = \begin{cases} \alpha_{i} \Delta_{i}, F(mode, sgn(s_{i-1})sgn(\sigma)sgn(x_{i})) = +1 \\ 0, F(mode, sgn(s_{i-1})sgn(\sigma)sgn(x_{i})) = -1 \end{cases}$$
(9)

for i = 2, ..., n, in which F is given by

$$F[mode, l(t)] := \begin{cases} l(t), mode = "Hard-Switching" \\ l\left(\left\lfloor \frac{t}{T_s} \right\rfloor T_s\right), otherwise \end{cases}$$
(10)

Furthermore, suppose Δ_i and α_i in turn satisfy

$$\Delta_i = \begin{cases} 1, mode="Hard-Switching" \\ 0, mode="No-Switching" \end{cases}$$
(11)

with $\Delta_i \in (0, 1)$ if mode = "Mild-Switching", i = 1, ..., n, and

$$\alpha_i = -\frac{s_{i-1}}{s_i} - c_i, \ c_i > 0, \tag{12}$$

for i = 2, 3, ..., n. Then if x(0) is chosen such that $|\sigma(0)| < \rho$, the modulator is stable in the sense that ||x(t)|| is bounded and $|\sigma(t)| < \rho$ for all $t \ge 0.\square$

Proof (sketch):

We first show that with the system described above, finite-escapetime instabilities (described in [9]) cannot occur under the mild- or no-switching modes. Thus there is no danger than the system state will "blow up" to infinity before hard-switching can set in.

Since in mild- or no-switching, the switching feedback gains are time-latched, the right-hand side of H can be shown to be piecewise (in time) globally Lipschitz. Thus, using [9, Theorem 2.3], it can be shown that the solution x(t) exists for all time. Therefore there are no finite escape times.

We now show that under hard-switching, from any initial state $x(0) \in \mathbb{R}^n$, $x(t) \to 0$ such that $|\sigma(t)|$ decreases monotonically from $|\sigma(0)|$. We define our positive definite Lyapunov-like function as

$$V(\sigma) = \frac{1}{2}\sigma^2.$$
 (13)

Recall that $\sigma = \Sigma_0 x$. Note that for this Lyapunov argument, we assume that $\sigma \neq 0$, and fix the system in hard-switching mode. Differentiating (13) with respect to t yields

$$\dot{V} = \frac{dV}{d\sigma} \frac{d\sigma}{dx} \dot{x}$$

$$= s_1(k_1)\sigma x_1 + \sum_{i=2}^n s_i (\frac{s_{i-1}}{s_i} + k_i)\sigma x_i$$

$$+ s_n \sigma (\delta \operatorname{sgn}(\sigma) + r).$$
(14)

After some manipulation, we obtain

$$\dot{V} < s_1(k_1)\sigma x_1 + \sum_{i=2}^n s_i (\frac{s_{i-1}}{s_i} + k_i)\sigma x_i + s_n |\sigma| (\delta + |r|_{\infty}).$$
(15)

Now, by inspection of this inequality, it can be seen that if δ and k_i , i = 1, ..., n, are given by (8) and (9) in the hard-switching mode, then

$$V < 0, \ \sigma \neq 0. \tag{16}$$

From [6, Theorem 1], the hyper-plane $\sigma = \Sigma_0 x = 0$ contains a globally reachable sliding mode. On the surface $\sigma = 0$, the modulator state evolves according to the dynamics

$$D_{\sigma}: \quad \frac{\dot{x} = [I - B_0(\Sigma_0 B_0)^{-1} \Sigma_0] A_0 x}{\Sigma_0 x = 0}$$
(17)

specified by the method of equivalent control [11]. It can be shown that the eigenvalues of $[I - B_0(\Sigma_0 B_0)^{-1}\Sigma_0]A_0$ correspond to the zeros of the nominal loop filter, H_0 . But since H_0 is minimum phase, D_{σ} is stable.

Thus, for any initial state x(0), the system is stable in the sense that ||x(t)|| and $|\sigma(t)|$ are bounded. Moreover, since $\dot{V} < 0$ and $V = \frac{1}{2}\sigma^2$, $|\sigma|$ cannot increase with time under hard-switching. Therefore, quantizer overload is prevented if ρ is chosen sufficiently small. \Box

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