RASSP: METHODS AND TOOLS FOR RAPID SIGNAL PROCESSOR DEVELOPMENT, UPGRADING AND LIFE CYCLE SUPPORT

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ABSTRACT

The Rapid Prototyping of Application Specific Signal Processors (RASSP) program is an ARPA/Tri-Service initiative intended to dramatically improve the process by which complex digital systems, particularly embedded digital signal processors, are designed, manufactured, upgraded, and supported. RASSP seeks to improve by at least a factor of four (4x) the time required to take a design from concept to fielded prototype. RASSP is motivated by the need to provide affordable embedded signal processors for a wide range of DoD systems that are state-of-the-art when they are fielded, rather than when they are first defined.

1. RASSP FOCUS

Achieving the RASSP program goals will require a coordinated approach to signal processor architecture; design methodology; and electronic design infrastructure (see Figure 1), which includes such items as Electronic Design Automation (EDA), reuse libraries, and enterprise networking. Keeping the program tractable requires a strong focus on a specific problem domain. Determining whether the program goals have been met will require a comprehensive approach to evaluation of the RASSP design environment.

It is also important to realize that RASSP is not focused on the design of application specific integrated circuits (ASICs) or even of board-level products. Instead, RASSP is focused on the design of larger electronic systems that will typically encompass multiple boards, a variety of implementation technologies and interfaces, and a wide range of data rates.

1.1. RASSP Design Methodology

Two major components of the design methodology being explored by the RASSP developers are top-down, concurrent design and the model year concept. The RASSP design methodology evolves from a top-down approach, similar to traditional system

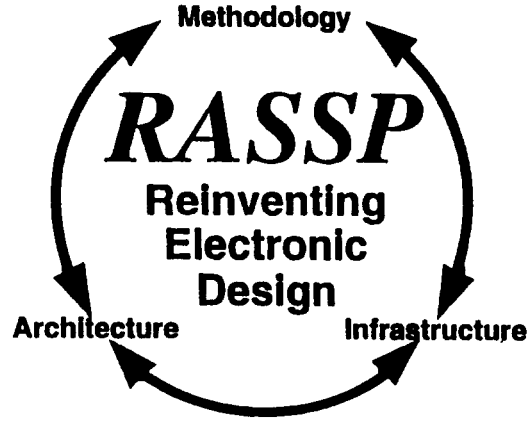

Figure 1. The RASSP program combines research in signal processor architecture, design methodology, and design automation tools.

engineering techniques that begin with a formal specification which is successively refined to greater and greater levels of detail in a modified "waterfall" or more commonly known as the spiral process until the complete design is finalized. In RASSP, the traditional paper specifications will be replaced in part by computer simulatable specifications as a means of ensuring correctness and removing ambiguities. RASSP further updates the top-down model by applying concurrent engineering concepts along with a model year concept.

1.1.1. Model Year Concept

RASSP advocates an alternative "model year" based design methodology which depends on a successive refinement approach. This method, represented by the lines marked "MY1" ("model year 1") through "MY4" in Figure 2, builds an initial design based on a subset or relaxed set of specifications, primarily using existing hardware and software technology. The resulting prototype can be delivered to the user for test and evaluation much more quickly. The design is then upgraded, using refined user

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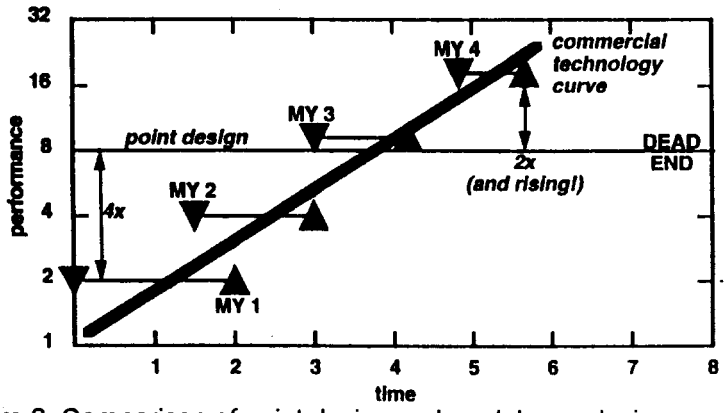

Figure 2. Comparison of point design and model year design approaches.

requirements and inserting more recent technology. In the same total amount of time required to field the point design, the model year approach may evolve through several design cycles.

The model year methodology assumes the performance of available commercial technology improves rapidly, as indicated by the "commercial technology curve" in Figure 2. So long as this remains true, a model year design approach which substitutes several short design cycles for one long cycle will end up with better performance than the point design, even if the initial baseline design must sacrifice some desired performance. Improved performance is achieved with much less reliance on expensive, difficult-to-support custom hardware and software.

The user gains from the model year approach in several ways. He or she obtains a higher-performance signal processor as a lower design cost. The processor has lower life cycle support costs because it is based on standard technology and can be upgraded as required to track commercially available technology. The user also is provided prototype hardware and software early and often, by way of the evolving model year prototypes. This provides a means for uncovering flaws in the system specifications while they are still correctable, resulting in an ultimate product better suited to the user's needs. The user becomes part of the development process in the RASSP model year design paradigm.

The model year design methodology will not be efficient unless each design cycle is able to build upon the previous cycle; each model year must not start from scratch. To achieve that, the processor architecture must promote modular design and re-use of hardware and software, allowing upgrades of portions of the processor without requiring re-design of the entire system. These lessons have long been understood in the software community; RASSP seeks to apply the same concepts to embedded hardware

Consequently, the "RASSP" architecture is a set of concepts describing a flexible approach to designing DSPs, including scalability, heterogeneity, life cycle support, flexible interfaces, modularity, and testability.

1.2. RASSP Architecture

"The" RASSP architecture is not a particular processor design, but rather a set of concepts describing a flexible approach to designing DSPs. These include scalability, heterogeneity, life cycle support, flexible interfaces, modularity, and testability.

While the RASSP focus on embedded DSPs does constrain the range of designs which must be considered, that range is still considerable. RASSP architectural ideas must therefore be scalable to span a range of performance requirements from a few MFLOPS to tens, even hundreds, of GFLOPS.

Architectural subsystems are connected with interconnect fabrics (wires, buses, crossbars, fiber optic lines, etc.) based on scalable, open hardware designs and software communication protocols. Note that the interfaces to the sensor at one end and to displays or data processors at the other will generally be beyond the control of the RASSP designer, emphasizing the need for flexibility in interface capabilities. This approach of modularized hardware with standard interfaces between modules localizes the influence of a change in the design of any one portion of the system.

The architectural requirements for life cycle support reflects two major concerns: upgradability and testability. Upgradability will be ensured through the use of modularity of hardware and software and flexible interfaces in a model year design framework. Extensive hierarchical testability will be designed in from the start as part of the concurrent engineering thrust to improve product quality and reduce the cost of field maintenance and support. However, the RASSP testability approach must be flexible enough to incorporate the varying degrees of built-in-test that come with the decision to use off-the-shelf parts where feasible.

1.3. RASSP Infrastructure

The RASSP infrastructure [design environment] will support all aspects of embedded DSP development, from program management through detailed design and assessment to manufacturing and logistics support. The design environment integrates numerous tools, such as: requirements capture, program management, high level synthesis tools; design methodology managers; library managers with their design libraries; and file managers. The challenge is to develop this design environment; making it easy for all parts of the design environment to communicate and manage data; and, at the same time, making it user friendly while using , for the most part, commercially available tools.

The basic concept of operation of the design environment is based on implementing workflows. The methodology or work flow manager controls the execution of the RASSP development process by guiding the user through the appropriate steps of the DSP design process from requirement capture to manufacturing. The work flow manager automatically invokes the tool and, when necessary, the tool's appropriate data format translators.

2. RASSP PROGRAM STRUCTURE

RASSP is an ARPA/Tri-Service managed program. The current ARPA program manager is Dr. Mark A. Richards. All program participants draw upon the existing EDA and DSP industrial infrastructure for independent development and products.

2.1. RASSP Primary Developers

The two primary development contractors ("primes") are at the center of the RASSP program. Each of the primes is responsible for development, integration, and demonstration of a comprehensive RASSP design environment.

This includes development of a suitable:

- signal processor architecture
- cost and "ility" models
- design methodology
- manufacturing interface
- virtual prototyping methodology
- technology insertion plan
- design for testability methodology
- technique for inheriting legacy systems
- RASSP data base
- business plan

and other tasks as necessary.

Teams led by Lockheed Sanders, Inc. (Nashua, NH) and Martin Marietta Advanced Technology Laboratories (Moorestown, NJ) were selected as primary development contractors and began work on July 30, 1993.

2.2. RASSP Technology Base Program

At the start of the RASSP Program, there were a number of specific areas where technology was not advanced enough to meet RASSP requirements. To meet this need, there were a number of Technology base development contractors who are responsible for developing or accelerating specific EDA technologies or standards which can then be used by the primary development contractors, either directly or through adoption into EDA vendor products. The first ten RASSP technology base awards were made in mid 1993 primarily to universities, followed by an additional ten, in mid 1994, primarily to industry.

2.3. RASSP Benchmarking

Assessment of the improvements made possible by the RASSP paradigm is an important aspect of the RASSP Program. Therefore, the benchmarking contractor is responsible for designing, administering, and evaluating a series of semiannual design exercises. This contractor is independent of both the primary development and technology base contractors, and is experienced with both embedded signal processor design and DoD applications. The Massachusetts Institute of Technology's Lincoln Laboratory (MIT/LL) was selected for this role.

2.4. RASSP Education/Facilitation

To accelerate technology transfer, the RASSP Program has enlisted an Educator/Facilitator (E/F) contractor to play the leading role in this technology transition process.

This contract was awarded to an industry/university team led by the South Carolina Research Authority (SCRA) in June 1994.

The E/F is an independent contractor who serves as a source of knowledge about the RASSP design environment and its performance.
A second key role for the E/F is to provide information and technical support services to third party users and vendors concerning benchmark results, establishment of RASSP design capabilities, and training of users through such mechanisms as user briefings, workshops, tutorials, and engineering support services.

2.5. RASSP Demonstrations

TRW will demonstrate and validate the Martin Marietta RASSP methodology and infrastructure by developing an integrated communication, navigation and identification (CNI) system. Targeted toward the Comanche CNI subsystem, the demonstration system will provide greater flexibility as well as improved performance. This system will allow waveforms and functions to be added as CNI system requirements change.

Hughes will demonstrate the success of Lockheed's RASSP design environment (RDE) by upgrading the Infrared Search and Track (IRST) signal processor currently in use on the Navy's F-14D. Anticipated benefits of the demonstration system will include a dramatic improvement in clutter suppression as well as allowing low cost algorithm upgrades in the future.

In addition to the above demonstrations there are two other demos in process. These include an acoustic sonobuoy upgrade and a classified signal processor upgrade.

2.6. Getting Involved With RASSP

The E/F contractor is responsible for disseminating all RASSP information to the public. You may reach the E/F in any of the following ways:

(a) RASSP World Wide Web - http://rassp.scra.org
(b) FTP - ftp.rassp.scra.org
(c) email - info@rassp.scra.org
(d) phone - (803) 760-3376 POC Anthony Gadient

References:

[1]. Proceedings of the 1st Annual RASSP Conference, August 1994.