INTRODUCTION TO ARPA'S RASSP INITIATIVE AND EDUCATION/FACILITATION PROGRAM

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ABSTRACT

The Rapid Prototyping of Application Specific Signal Processors (RASSP) U. S. Department of Defense (ARPA/Tri-Services) initiative is intended to dramatically improve the way digital systems, particularly embedded digital signal processors, are designed, manufactured, upgraded, and supported. These DSP systems are complex, with typically one or more printed circuit boards, a variety of implementation technologies and interfaces, and a wide range of data rates.

The target RASSP improvement is at least a fourfold (4x) reduction in the time to go from design concept to fielded system. Equivalent improvements in cost and quality are also targets. The motivation for the RASSP initiative is the pervasive need for affordable embedded signal processors throughout a wide range of DoD systems, signal processors that are state-of-the-art when they are fielded rather than when they are first defined.

A number of programs are included in the RASSP initiative. This paper introduces the initiative from both technical and programmatic viewpoints.

1 RASSP TECHNICAL APPROACH

The overall RASSP technical approach [1] is to coordinate improvement efforts in signal processor architecture, design methodology, and electronic design infrastructure. The infrastructure includes such items as Design Automation, reuse libraries, and enterprise networking and integration.

1.1 RASSP Signal Processor Architecture

The RASSP architecture [5] focus is on scalable, modular, and reusable architectures. With modular architectures, increased system capabilities can be obtained by replacing a component of a fielded system with a higher performing component without changing the rest of the RASSP system. With scalable architectures, increases in system capabilities can be achieved by adding additional copies of existing parts of a fielded RASSP system. In addition, RASSP architectural ideas must also be scalable to span a range of performance requirements from a few million operations to hundreds of billions of operations. To achieve these effects, the RASSP architecture approach has three primary targets: programmable embedded hardware, embedded software, and standard interfaces.

Software and hardware component interfaces must be defined to minimize the impact on other components if either a hardware or software component is changed or replaced. Notable RASSP interface characteristics are medium independence, wide use within industry and scalability. The RASSP interconnect fabrics (e.g., wires, buses, crossbars, fiber optic lines) are based on scalable, open hardware designs and software communication protocols. The interfaces to the DSP system input and output will generally be beyond the control of the RASSP designer, emphasizing the need for interface flexibility.

1.2 RASSP Design Methodology

The RASSP approach to design methodology is to capitalize on development improvement techniques that have been widely explored. These techniques include: concurrent engineering, top-down and spiral design, and simulation-based design methods such as virtual prototyping and executable specifications (2). In RASSP, the effort is to bring these techniques together in a consistent methodology that is integrated with both the automation infrastructure and the signal processor architecture approaches. Efforts have been focussed on filling the gaps that have kept these techniques from being widely used.

One lesser-known method that RASSP is based on is the Model Year concept, a successive refinement approach. This method builds an initial baseline design using a relaxed set of specifications, primarily with existing hardware and software technology. The resulting prototype can be delivered to

0-7803-2431-5/95 $4.00

the user for test and evaluation much more quickly. The design is upgraded, correcting any functional errors and inserting more recent technology. The model year method thus capitalizes on the rapidly improving performance of commercially available technology.

The user gains from the RASSP approach in several ways. First, a higher-performance signal processor is developed at a lower design cost. Second, the processor has lower life cycle support costs because cost is part of the early design evaluation and because the design is based on standard technology and can be upgraded as required to track supportable technology. Third, the user also is provided prototype hardware and software early and often. This provides a means for uncovering flaws in the system specifications early, resulting in a product better suited to the user's needs. With RASSP, the user becomes part of the development process in the RASSP model year design paradigm.

1.3 RASSP Design Automation Infrastructure

The RASSP initiative is expanding on commercially available Electronic Design Automation (EDA) capabilities to develop the comprehensive and integrated EDA capabilities needed to support RASSP improvement goals.

RASSP is relying on the VHSIC Hardware Description Language (VHDL) as a unifying design representation language and for tool integration. RASSP is exploring the feasibility of using VHDL-based simulation specifications(4) as part of the design and test specification of both hardware and software. To maximize the utility of this VHDL design and test specification, RASSP expects virtual prototyping to be used at each design stage to explore design options. Virtual prototyping requires hardware and software co-simulation technology, including: the ability to mix different computation models (for example, synchronous data flow and discrete event tokens); and the ability to have simulation tools, emulators, and hardware interact through simulation backplanes. RASSP is exploring advances in VHDL simulation technology and methodology to provide the tremendous simulation power demanded by virtual prototyping.

The RASSP design environment will include many high-level systems engineering EDA tools such as: pricing, design advisors to support early architectural decisions, tools for specialty analyses (e.g., manufacturability, reliability, maintainability), documentation and report generation. The RASSP design environment will also provide mechanisms to: integrate these high-level tools with tools used later in the design process, provide guidance on how to use the collection of tools in the context of the selected design methodology, and provide the linkage between business and technical data needed for configuration management of the technical data. The integration mechanisms will be based on standards, including VHDL, STEP and CFI.

1.4 Design Exercises

To evaluate and steer the RASSP efforts, an extensive set of design tasks is included. The design tasks are intended to exercise the RASSP design environment early and often on real problems covering a wide range of architectures, applications, and performance levels. Both system demonstrations and benchmarks are included.

System demonstrations are specific processor designs, proposed and performed by the primary development contractors, intended to be usable in a DoD weapon system. Demonstrations proceed through two to four model year cycles, resulting in prototype hardware and software suitable for testing in a fielded system. Demonstrations provide a low cost way for third parties (e.g., DoD program offices or other federal agencies) to participate in the RASSP program by funding a design of their own specification.

Benchmarks are more modest and more generic but still involve DoD-relevant designs. Benchmarks will result in products in either virtual or actual form. The RASSP benchmark contractor will verify that the products meet specification, but the real thrust of this program activity is to collect benchmark information on the design *process* used to create the product. Six semiannual benchmark designs are planned for the RASSP program.

2 PROGRAM STRUCTURE

The RASSP program is managed by the ARPA Program Manager, who is supported by representatives of each of the Services. The current ARPA program manager is Dr. Mark A. Richards. All program participants draw upon the existing EDA and DSP industrial infrastructure for independent development and products.

2.1 Primary Development and Demonstration

The primary development contractors (primes) are at the center pieces of the RASSP initiative, responsible for development, integration, and demonstration of a comprehensive RASSP design environment. The primes also carry out the semiannual benchmark and system demonstration design exercises.

Teams led by Lockheed Sanders, Inc. (Nashua, NH) and Martin Marietta (Moorestown, NJ)

were selected as primes and began work on July 30, 1993. While both subscribe to the basic RASSP concepts described previously, the two primes differ significantly in their approach to architecture, design environment development, and methodology. Annual releases of their respective RASSP Design Environments are planned by the primes, nominally in early summer of each year 1994 through 1997. These design environments will initially be released to evaluation sites associated with each developer's program. The prime's substantial accomplishments are described in [1] through [5].

2.2 Technology Base Development

The goal of the RASSP Technology Base (tech-base) Research and Development programs are to provide significant advancements beyond the current generation of design automation technology. These programs are developing or accelerating specific EDA technologies or standards that can then be used by the primes, either directly or through adoption into EDA vendor products. These tech-base efforts will provide models where there are none available and automation to areas where manual methods are current practice. The set of programs is quite diverse but they follow a small set of themes including:

1) Innovative algorithms for digital signal processing (University of Minnesota and Massachusetts Institute of Technology).
2) Advanced design synthesis technology (University of Cincinnati, University of Minnesota, and Logic Vision Software)
3) Hardware/software co-design and high level system trade-off tools (University of California - Berkeley, University of California - Davis, University of Virginia, Carnegie Mellon University/University of Oregon, Research Triangle Institute/Virginia Polytechnic Institute, Honeywell, Omniview, JRS Research, GM-Hughes, and Management Communications and Control Inc.)
4) Design automation infrastructure support (University of Cincinnati, CAD Framework Initiative, and Intermetrics).
5) The development of public domain VHDL models (Georgia Institute of Technology, Mississippi State University, and Ohio State University).

2.3 Benchmarking

Massachusetts Institute of Technology's Lincoln Laboratory (MIT/LL), as the benchmarking contractor, is designing, administering, and evaluating the semiannual design exercises. In this program, MIT/LL is applying expertise in embedded signal processor design and DoD applications to provide exercises developed by a source independent of any of the other RASSP programs.

While MIT/LL must verify compliance of each benchmark design with the specifications, the more important function is to evaluate the design process which created that design. A significant challenge is therefore defining quantifiable metrics for the integrated design process.

The approach being applied to the first benchmark design, expected to evolve throughout the RASSP initiative, is based on two distinct classes of metrics. The first class of metrics includes those used in commercial parametric cost estimators (PCEs). PCEs are being calibrated for each prime's design process, used to establish a pre-RASSP (July 1993) design process baseline, and to predict the life cycle implications of RASSP design improvements. The second metrics class includes direct measures of design process and product complexity. Design process metrics are aimed at measuring such items as hardware and software re-use, requirements traceability, tool productivity and ease of use. Product complexity metrics address such issues as software size and complexity, or hardware performance, complexity, cost, and testability.

2.4 Technology Transition

Another important RASSP goal is to ensure that the design environment, methodology, and architectural approaches become adopted by the signal processing community and continue to evolve after the program is completed. The RASSP program has enlisted a novel Educator/Facilitator (E/F) contractor to play the leading role in this technology transition process. This contract was awarded in June 1994 to a team led by SCRA.

The E/F program serves as an education and information source about RASSP technology. The E/F acts as an emissary both between program players and the broader user and EDA communities. For example, the E/F serves as a public single point of information about status and plans of all RASSP activities. A variety of modern multimedia mechanisms such as Mosaic servers, bulletin boards, ftp sites, newsletters are being used to distribute this information and public domain RASSP simulation models and integration software.

A second key role for the E/F is to provide

information and technical support services to third party users and vendors concerning benchmark results, establishment of RASSP design capabilities, and training of users through such mechanisms as user briefings, workshops, tutorials, and engineering support services. The E/F team will also monitor the experiences of third-party RASSP users, feeding back lessons learned to the RASSP steering committee and developers. User training mechanisms include workshops, tutorials, and engineering support services.

The third important E/F role is the development of university curricula, continuing education courses, and learning aids so that RASSP design technology can be introduced to undergraduate and graduate students and to working engineers and managers.

For more information, access the RASSP MOSAIC Server (3), send email to *info@rassp.scra.org* or call 803-760-3376.

2.5 Accomplishments

The RASSP program is one and one-half years old, about one-third of the way through. Even at this early stage, there have been a number of concrete accomplishments.

First, a considerable achievement on the part of the ARPA/Tri-Service team is the completion of the RASSP procurements with 25 prime contracts and a large number of subcontractors.

The primary developers, Lockheed and Martin Marietta, have each established working virtual corporations for collaborative design and communication. They have developed, installed, and integrated baseline RASSP design environments, and begun definition and implementation of their respective top-down, standards-based design methodologies. Each developer is also refining its own unique approach to DSP architecture and exploring the implications for processor design. Work has begun on the major demonstration projects, Lockheed's IRST processor and Martin Marietta's ICNI processor, and will soon begin on additional demonstrations. Finally, the primes have established working relationships, both formal and informal, with a "who's who" of the electronic design automation industry and are beginning to explore business approaches to the problem of maintaining, evolving, and disseminating RASSP design technology after the RASSP program itself is complete.

As discussed above, MIT/LL has defined the first benchmark application thread and has developed the written and executable specifications for the first and second benchmark cycle. The executable specification effort is proving of special interest and value in exploring the issues involved in applying VHDL at this level. In addition, MIT/LL has defined an initial approach to benchmarking an entire design process and a comprehensive set of cost, process, and product metrics.

The twenty technology base programs can claim many achievements to date. A sampling of these includes:

- Analysis of the pros and cons of a variety of DSP algorithm development tools,
- Substantial progress in the Ptolemy system-level design and simulation tools,
- Substantial progress in the TIBBIT system for retargeting of legacy software,
- A draft VHDL-based specification language incorporating area, speed, and power constraints,
- Progress in developing a tool for analyzing the complexity of MATLAB scripts,
- Acceleration and extension of standards needed to support tool integration,
- Initiation of the development of VHDL library models for common microprocessors.

The RASSP E/F program, launched in June of 1994, has established the RASSP Information server. E/F has defined a draft education plan and developed several education modules for university graduate students and industrial technical staff and managers. Finally, the E/F program has initiated a quarterly RASSP newsletter, *The RASSP Digest*.

There are many other accomplishments which have been achieved by the participants in the RASSP Program. The initiative appears well on its way toward its fourfold improvement goal.

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