Real-time RLS-MLSE equalizer implementation for application to PDC (Personal Digital Cellular)

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ABSTRACT

This paper investigates the experimental performance of the recursive least square adaptive algorithm-maximum likelihood sequence estimation equalizer (RLS-MLSE) implemented in a single DSP for application to the Japanese PDC (Personal Digital Cellular) system under a harsh frequency-selective-fading environment. Frame synchronization and automatic frequency control (AFC) play important role to make the equalizer effective, because the performance impairment of those functions causes serious degradation of the equalizer performance. In order to improve total system performance under frequency-selective-fading, we apply a new high precision frame synchronization scheme using recursive least square(RLS) algorithm and also a new AFC algorithm scheme taking advantage of a replica of distorted unique word (UW). In the Rayleigh faded two-wave model with one symbol delay, 1% BER can be achieved at Eb/N0 equal to 16.0 dB with a maximum Doppler frequency equal to 40 Hz.

Table 1. The parameters of the experimental systems

RF frequency	900MHz
Multiple access scheme	3 channel TDMA
Transmission bit rate(total)	42kbps
Modulation scheme	$\pi/4$ shifted DQPSK
Frame length	140 symbols/frame
Unique word length	10 symbols/frame

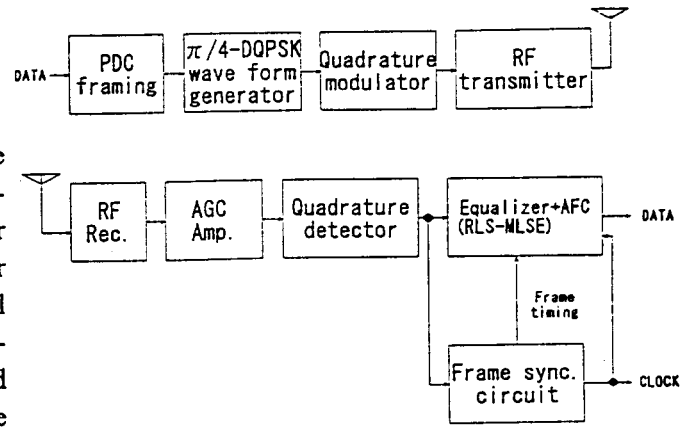

Figure 1. System blockdiagram

1. SYSTEM DESCRIPTION

Table 1 shows the parameters of the experimental system. We adopted RLS-MLSE algorithm(3) for real-time implementation using one-chip Floating-Point arithmetic DSP, which is suitable for fast time-varying channels. Figure 1 shows a system block diagram. At the transmitter, the input data sequence (11.2kbps) conformed to the PDC format and is transmitted using an assigned time slot. I(Inphase) and Q(Quadrature) baseband signals are generated according to $\pi/4$ shifted DQPSK modulation scheme with root Nyquist filtering and fed to a quadrature modulation. At the receiver, the received RF signal is down converted, and the I and Q baseband signals are obtained at quadrature detector after suppression of the envelope fluction into a proper dynamic range by AGC. Those detected I and Q baseband signals are converted from analog to digital, and are supplied to the frame synchronization circuit and equalizer which, after AFC processing, demodulates the modulated signal. The frame timing

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(50 Hz) and bit clock(for codec 11.2kHz) are extracted at the frame synchronization circuit.

2. EQUALIZER STRUCTURE

We adopted RLS-MLSE algorithm for real-time implementation using single-chip floating-point arithmetic DSP, which is suitable for fast time-varying channels. Figure 2 shows the configuration of RLS-MLSE process. In RLS-MLSE, the equalization is realized as the process of identifying the optimal state sequence, or detecting the optimal symbol sequence together with the simultaneous estimation of channel parameters . There are two channel parameter estimation phases. They are firstly a training phase where the estimation is performed using a unique word(UW, positioned at the center of burst frame) as a training signal and secondly a tracking phase where the estimation is continued using symbol sequence candidates. The sequence of symbols is transformed into I and Q baseband signals as a replica through T spaced transversal filter representing the relevant channel impulse response corresponding to each state. The difference between the received I and Q baseband signals and the replica constitutes the estimation error. This transversal filter is adaptively controlled by a parameter estimator through the tap coefficients so as to minimize the estimation error using RLS algorithm. The sequence with minimum estimation error is selected by the MLSE controller using Viterbi algorithm.

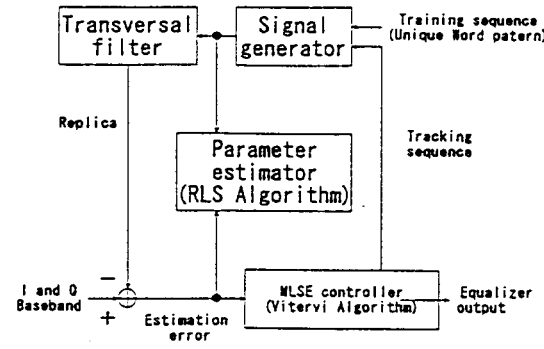

Figure 2. Configuration of RLS-MLSE

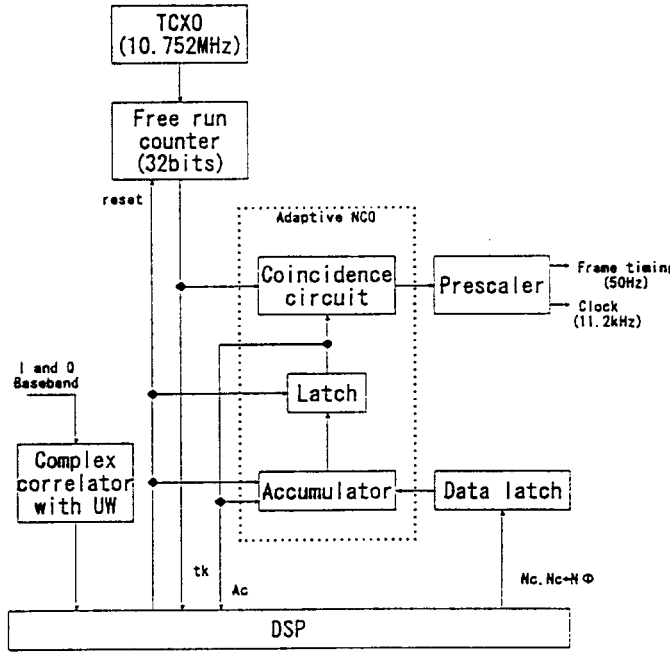

Figure 3. High precision synchronizer blockdiagram

3. HIGH PRECISION SYNCHRONIZATION

Carrier frequency offset and fast fading with delay spread cause a considerably large timing jitters which induces equalizer performance degradation. Therefore, high precision timing synchronization is necessary to improve the BER performance under harsh frequency-selective-fading. Figure 3. shows the configuration of the newly developed high precision synchronizer. The frame timing and bit clock are recovered by means of detecting the UW timing in each slot. The peak absolute value of the complex correlation between the received I and Q baseband signals and the UW signal pattern is detected through complex correlattor, and fed to DSP.

The DSP detects the rough frame timing by means of detecting the peak of the complex correlation, and measures the frame period (tk) using a 32 bit free run counter. Through the measurement, the DSP, using RLS algorithm, estimates clock cycle factor (Nc) and phase adjustment factor (Nc+N ϕ) for adaptive NCO (Numerical Controlled Oscillator) which consists of an accumulator ,latch ,and coincidence circuit. The adaptive NCO is preset with those estimated parameters and outputs the gross rate of the bit clock of

33.6 kHz precisely synchronized with the transmitter clock. The prescaler produces frame timing signal(50 Hz) and the bit clock(11.2 kHz) for demodulation by dividing the 33.6 kHz clock. Thus the synchronizer shown in Figure 3 provides the timing recovery with a high stability, precision, and speed under multipath fading.

4. AFC

AFC is performed by means of digital signal processing prior to adaptive equalization. Figure 4 shows a configuration of the AFC. The complex correlation between the differential sequences taken from the received I and Q baseband signals and that of the UW provides the carrier frequency offset information between the transmitter and receiver, because the amount of the received signal vector rotation during UW due to the offset appears in the given complex correlation value. Therefore the estimated frequency offset factor F can be obtained by averaging the complex correlation value. Frequency offset compensation is accomplished by an inverse rotation of the received signal vector represented by I and Q signals by F*, where * denotes complex conjugate. However, using the UW pattern which is fixed and not long enough sometimes results in a considerable frequency offset factor estimation error, caused by the residual correlation of delay paths under a multipath fading environment. Therefore we applied the new AFC method taking advantage of a replica of distorted UW. The AFC consists of inverse rotator for frequency compensation, a correlator to recover transmitted carrier through the correlation between received UW and a replica of distorted UW, and an offset frequency estimator to estimate the offset from recovered carrier.

5. EXPERIMENTAL RESULTS

Figure 5 shows an experimental result of the equalizer BER performance with a parameter of maximum Doppler frequency f_D =160, 80, 40, 5 Hz in the Rayleigh faded two-wave model (τ_d = 1T, D/U ratio = 0dB), using the high precision synchronizer and AFC.

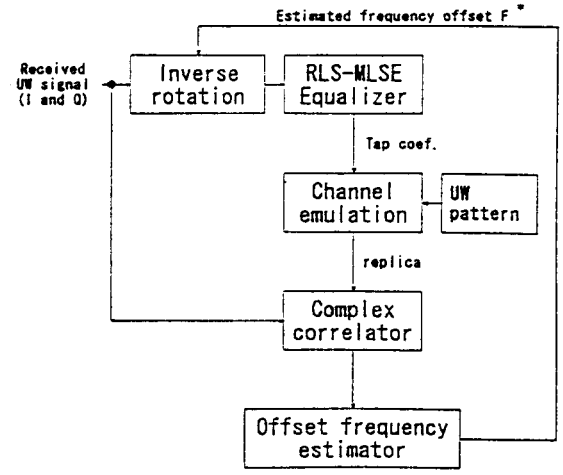

Figure 4. Configuration of AFC

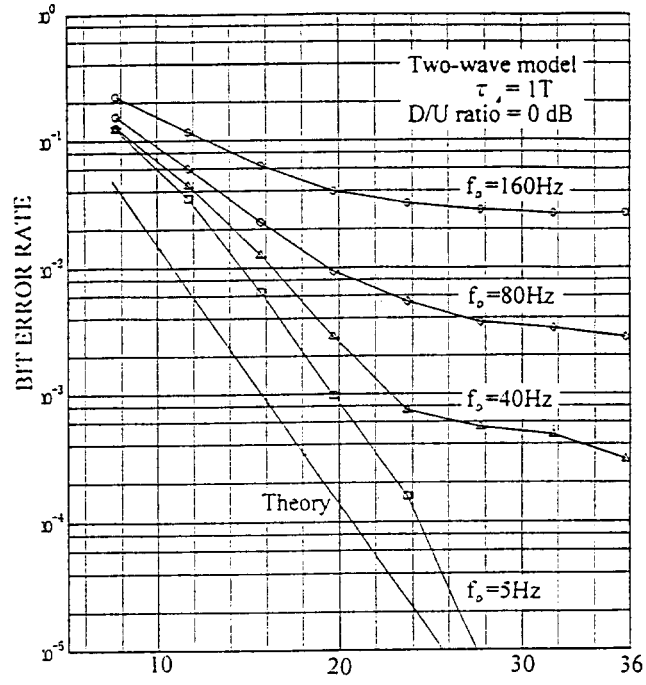

Figure 5. BER performance of RLS-MLSE equalizer

The theoretical average BER is given by $3/2(E_b/N_0)^2$,which is equivalent to that of two branch maximal ratio combining diversity for differential detection. The result shows that the average BER becomes less than 10^{-2} for an average E_b/N_0 over 16 dB with f_D below 40 Hz. The degradation from theoretical value is approximately 4 dB for $f_D = 5$ Hz. This degradation includes timing error of synchronization and AFC estimation error under frequency-selective-fading.

Figure 6 shows BER performance versus the frequency offset with/without AFC. The experimental condition is as follows, average E_b/N_0 =24 dB, maximum Doppler frequency f_D = 80 Hz in the Rayleigh faded two-wave model (τ_d = 1T ,D/U ratio = 0 dB). With the AFC, BER performance is mostly flat for frequency offsets within the range of approximately $\pm$2.2 kHz even in the multi-path-fading environment.

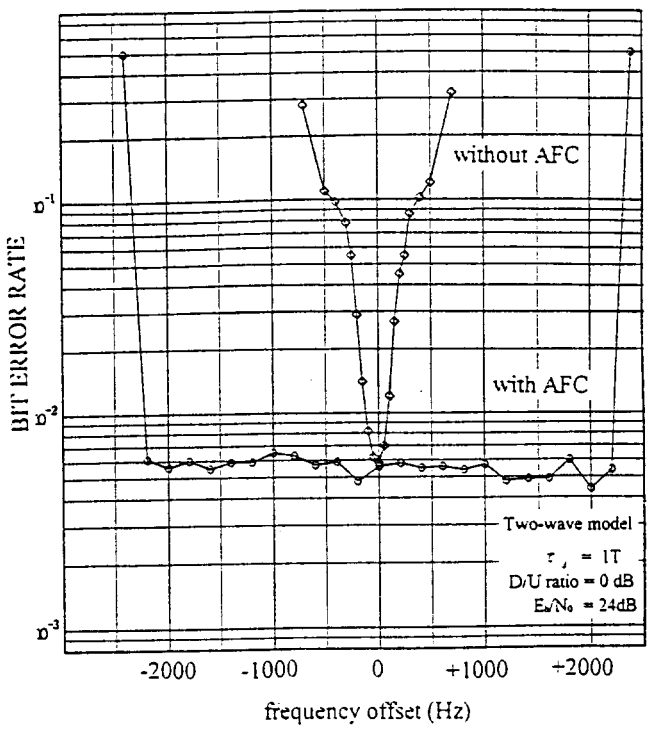

Figure 6. BER performance versus the frequency offset with/without AFC

6. CONCLUSION

We implemented real-time RLS-MLSE equalizer using single DSP which can overcome a harsh frequency-selective-fading environment utilizing new high precision timing synchronization and new AFC algorithm. In the Rayleigh faded two-wave model with one symbol delay, 1% BER can be achieved at E_b/N_0 equal to 16.0 dB with a maximum Doppler frequency equal to 40 Hz.

7. ACKNOWLEDGMENT

The authors would like to express thanks to members of Sendai Laboratory for their helpful discussions and contribution to the development.

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